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SOT-23 Micropower, Rail-to-Rail Op Amps Operate with Inputs above the Positive Supply

by Raj Ramchandani

Introduction

The only SOT-23 op amps featuring Over-The-Top™ operation—the ability to operate with either or both inputs above the positive rail—are the 55µA LT1782 and the 300µA LT1783. Over-The-Top operation is important in many current-sensing applications, where the inputs are required to operate at or above the supply. A wide supply voltage range, from 2.7V to 18V, gives the LT1782/LT1783 broad applicability. The guaranteed offset voltage of 950µV over temperature is the lowest of any SOT-23 op amp. There is even a shutdown feature for ultralow supply current applications.

General Purpose Appeal

The LT1782/LT1783 SOT-23 op amps are ideal for general-purpose applications that demand high performance. These SOT-23 op amps handle input voltages as high as 18V, both differential and common mode, independent of the supply voltage, making them ideal for applications with wide input range requirements and/or unusual input conditions. (For a description of the unique input stage that achieves this, see *Linear Technology* VIII:2, May 1998, p.10.) In applications that require more bandwidth than the 200kHz LT1782, the LT1783's sixfold increase in supply current gives it six times more bandwidth and slew rate. The LT1782/LT1783 are available in two pinouts: a 6-lead version with a shutdown feature that reduces supply current to only 5µA and a standard-pinout 5-lead version. Table 1 summarizes the performance of these new op amps.

Read All of the Specs

The appeal of other SOT-23 op amps begins to diminish when the specifications are reviewed in detail. Common factors that keep most SOT-23 parts from being general-purpose amplifiers include low supply voltage range, high input offset voltage, low voltage gain and poor output stage performance.

To address these problems, the LT1782/LT1783 are fabricated on Linear Technology's "workhorse" high speed bipolar process, which allows the amplifiers to operate on all single and split supplies with a total voltage of 2.7V to 18V. For improved precision, thin film resistors are tightly trimmed at wafer sort; this guarantees that the input offset voltage will

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Issue Highlights

Our cover article for this issue introduces the LT1782/LT1783, the only SOT-23 op amps featuring Over-The-Top operation—the ability to operate with either or both inputs above the positive rail. Over-The-Top operation is important in many current-sensing applications, where the inputs are required to operate at or above the supply. A wide supply voltage range, from 2.7V to 18V, gives the LT1782/LT1783 broad applicability. The guaranteed offset voltage of 950µV over temperature is the lowest of any SOT-23 op amp.

In our Design Features section, we debut a new micropower, precision voltage reference: the new LT1461 bandgap voltage reference is a low dropout reference that has superb temperature coefficient, tight output tolerance and low supply current. High output current and unmeasurable thermal regulation make the LT1461 ideal for micropower precision regulator applications. To achieve these characteristics, new wafer trim techniques were developed and extensive characterization of thermal hysteresis and long-term drift were performed.

In the power realm, we present two new products: The LTC1759 Smart Battery Charger and the LT1306 synchronous boost converter. The LTC1759 is a Smart Battery Charger that offers constant-current (CC) and constant-voltage (CV), charging modes. The LTC1759 also incorporates such features as SMBus programmable output voltage and current, external, resistor programmable current limit, LTC's patented programmable AC wall adapter current limiting to maximize charge rate and efficiencies as high as 95%.

The LT1306 is a synchronous boost DC/DC converter with the ability to disconnect its output from its input in shutdown (traditional boost converters lack this ability). Additionally, the LT1306 can regulate the output when the input voltage exceeds the output voltage. This is useful, for example, for generating a 5V supply from a 4-cell alkaline battery. Lastly, inrush current is controlled, so a new battery can be installed without risking high inrush current as the battery initially charges the output capacitor.

Two new additions to LTC's Hot Swap™ controller family, the LTC1642 and LTC1645, are premiered in this issue. The LTC1642 limits the charging current drawn by a board's capacitors, allowing safe circuit board insertion into a hot backplane. It also offers additional capabilities, some new to the Hot Swap family: a maximum recommended operating voltage of 16.5V, a programmable electronic circuit breaker with foldback current limiting, overvoltage protection to 33V, and a voltage reference and uncommitted comparator.

The LTC1645's two channels can be set to ramp up and down separately at a programmable rate or they can be programmed to rise and fall simultaneously, ensuring power supply tracking at the two outputs. Two high-side switch drivers control the external N-channel FET gates for supply voltages ranging from 1.2V to 12V. Programmable electronic circuit breakers protect against shorts at either output.

Another new interface product is the LTC1755 smart card interface. The LTC1755 provides a simple and complete solution to smart card interfacing. Requiring only two bypass capacitors and one charge pump capacitor, the LTC1755 interfaces seamlessly between a smart card socket and a host microcontroller. It is designed to comply with all of the available electrical standards for smart card interfacing.

This issue offers a variety of Design Ideas, including a PolyPhase™ DC/DC converter that combines power from multiple inputs, an isolated RS485 transceiver, a sine wave to square wave converter using the LT1719 comparator and a tiny backlight power supply for palmtop devices, plus the third in a series of articles on designing filters with added stopband notches using the LTC1562 Operational Filter™ IC.

We conclude with six New Device Cameos.

LTC in the News...

On October 12, 1999, Linear Technology Corporation announced its financial results for the first quarter of fiscal year 2000. Robert H. Swanson, Chairman and CEO, stated, "Although the summer quarter historically has minimum growth, this was a strong quarter for us as demand from our customers continued strong, increasing in all major markets." The Company reported sales of $147,531,000 (a 5% increase over sales for the previous quarter) and net income of $58,457,000 compared with $44,382,000 a year ago. Net sales were up 27% over last year.

Immediately after first quarter earnings were released to the press, Linear Technology Chairman and CEO Robert H. Swanson was interviewed live on CNNfn's *Digital Jam* by commentator Bruce Francis. The interview focused on Linear's earnings and the forces driving the analog market. *Digital Jam* is received nationally in over 12,000,000 households.

The Company was featured in the *New York Times* in an article entitled "Analog's Success Stories." Linear Technology was touted as a "pure play" analog company that is an apparent paradox of the digital revolution. As Jill Hauser of T. Rowe Price observed in the story, "if anything, the digital phenomenon has increased demand, it has driven analog."

Barron's recently speculated in an article that Linear Technology might soon become one of the S&P 500 Index companies. The S&P is the most widely used benchmark for professional investors.

Table 1. LT1782/LT1783 SOT-23 guaranteed performance, V_S = 3V/0V or 5V/0V, T_A = 25°C

Parameter	LT1782	LT1783
Supply Voltage Range	2.7V to 18V	2.7V to 18V
Supply Current	55µA	300µA
Input Offset Voltage	800µV	800µV
Input Bias Current	15nA	80nA
Input Current, V⁺ = 0V (typ)	0.1nA	0.1nA
Input Offset Current	2nA	8nA
Open Loop Gain, RL = 10kΩ	200V/mV	200V/mV
PSRR	90dB	90dB
CMRR	90dB	90dB
Common Mode Range	0V to18V	0V to 18V
Output Swing, Low, Relative to V⁻	8mV	8mV
Output Swing, High, Relative to V⁺	90mV	90mV
Slew Rate (typ)	0.07V/µs	0.42V/µs
Gain Bandwidth Product (typ)	200kHz	1.25MHz
C_{LOAD} Stability (typ)	500pF	500pF
Input Noise Voltage (typ)	50nV/√Hz	20nV/√Hz
Input Noise Current (typ)	0.06pA/√Hz	0.14pA/√Hz

be under 950µV over the commercial temperature range. This results in the lowest offset voltage of any SOT-23 amplifier. Furthermore, unlike competitive amplifiers with meager open-loop voltage gains of 20V/mV or less, the LT1782/LT1783 have a guaranteed voltage gain of 200V/mV into a 10k load.

Finally, to optimize the output stage, nitride capacitors were added to the process. This halves the area of the internal compensation capacitors and allows small die size with excellent frequency stability. In fact, the LT1782/LT1783 are stable with capacitive loads up to 500pF under all load conditions. The minimum output stage current is ±18mA and the output swing is guaranteed within 8mV of ground and 90mV of the positive rail with no load. A problem encountered with other op amps in some applications is that as the output approaches the rail or ground, the gain degrades. The data sheet typically claims the output can swing to within a few millivolts of the rail, but the input overdrive required to achieve this can be quite high. This is not the case with the LT1782/LT1783; a few millivolts of input overdrive is enough to swing the outputs to their guaranteed value. Figure 1 shows the typical output saturation voltage vs input overdrive.

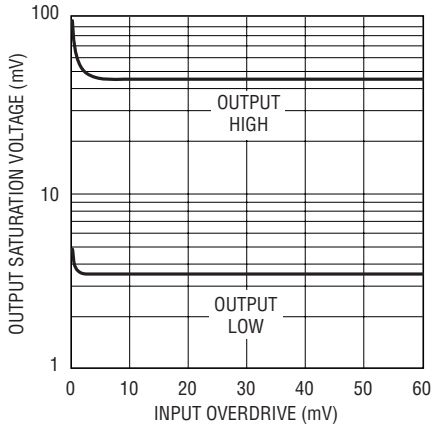

Figure 1. Output saturation voltage vs input overdrive

Other Niceties

Attention to small details is important for universal acceptance into general-purpose applications. The parts are completely specified on 3V, 5V and ±5V supplies and the op amps operate properly if the shutdown pin is left floating. Input-stage phase-reversal protection prevents the output from reversing phase when the input is forced up to 9V below the negative supply. Input protection resistors safely limit the current to less than 3mA when the inputs are forced to this extreme.

An Over-The-Top Sensing Application

The circuit of Figure 2 utilizes the Over-the-Top capabilities of the LT1782. The 0.2Ω resistor senses the load current while the op amp and NPN transistor form a closed loop, making the collector current of Q1 proportional to the load current. The 2k load resistor converts the current into a voltage. The positive input voltage, V_{BATT}, is not limited to the 5V supply of the op amp and could be as high as 18V. The LT1783 draws only 0.1nA of current through the inputs when it is powered down, extending the battery life.

Conclusion

Linear Technology's first SOT-23 op amps are not just space savers, they are tiny, tough and boast a variety of features that all join to make the LT1782/LT1783 truly general purpose amplifiers. These new products will enhance the superior line of operational amplifiers from Linear Technology.

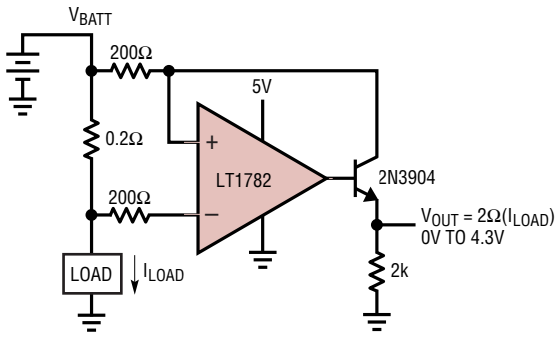

Figure 2. Positive-supply-rail current-sense application

3ppm/°C Micropower Reference Draws Only 50µA and Operates on 2.8V

by John Wright

Introduction

The new LT1461 bandgap voltage reference is a low dropout reference that has superb temperature coefficient, tight output tolerance and low supply current. In addition, high output current together with unmeasurable thermal regulation make the LT1461 ideal for micropower precision regulator applications. To achieve these characteristics, new wafer trim techniques were developed and extensive characterization of thermal hysteresis and long-term drift were performed.

How It's Done

At the heart of the LT1461 is the bandgap core: Q1, Q2, Q3 and Q4 of Figure 1. Q1 and Q2 generate a ΔV_{BE}, whereas Q3 and Q4 provide the attendant V_{BE}. The bandgap voltage is impressed across R1, and R2 provides gain for numerous voltage options. I1 provides patented curvature compensation that modifies the ΔV_{BE} current and greatly improves the temperature coefficient. High output current and excellent load regulation are the result of careful layout techniques and four betas of current gain from Q5 through Q8. The LT1461 has a shutdown control that can be used to turn off the reference during high output current conditions; it also has thermal shutdown or current-limit protection for the device during overload. Table 1 summarizes the performance specifications of the new reference.

How It's Really Done

In order for the factory to trim the output voltage to a very tight tolerance, four pins of the package are dedicated to trimming R1. This trim allows the LT1461 output voltage to be adjusted to better than 0.02%. The final specification, however, is a conservative 0.04%, because the part is measured with different factory testers and a safety margin or guardband is applied for thermal hysteresis.

The idea of this guardband is to ensure that the parts will remain 0.04% accurate even after they are exposed to temperature excursions of –40°C to 85°C. When a part is trimmed to high accuracy, its output voltage is valid only for the mechanical stress conditions that are present at the time of trim. The amount of stress will change with temperature because the thermal coefficient of expansion is different between the plastic package and the silicon chip. When the part returns to its "trimmed" temperature, there is no guarantee that the stress returns to exactly the initial amount, and the output voltage will be slightly different. This difference is called "thermally induced hysteresis shift" or "thermal hysteresis" and is expressed in parts per million (ppm). Figure 2 shows a distribution plot of thermally induced hysteresis shift on parts that were cycled several times between –40°C and 85°C. The LT1461 initial accuracy is specified broadly enough to include this hysteresis shift.

The output trim on the LT1461 uses all available pins on the package, so the temperature coefficient must be trimmed at wafer sort. If a reference has its bandgap voltage trimmed to the proper target or "bogie," it will have a near zero temperature drift. The problem is that the bogie moves with process variations and can differ from die to die. The solution is to measure the temperature coefficient at wafer sort and use an algorithm to correct the bandgap voltage. This requires wafer sorts at 75°C and 25°C to establish the drift. For example, if the bandgap voltage is trimmed to 1.2000V at 75°C and it moves 300µV to 1.2003V at 25°C, this corresponds to a –5ppm/°C drift. Once the TC is known, the bandgap voltage can easily be trimmed for zero TC by adjusting R3. The TC distribution widens when the parts are assembled in plastic because of stress on Q3 and Q4.

What the User Knows

Users encounter several problems when applying precision references and again thermal hysteresis is front and center. When a reference is soldered into a PC board, the elevated temperature and subsequent cooling

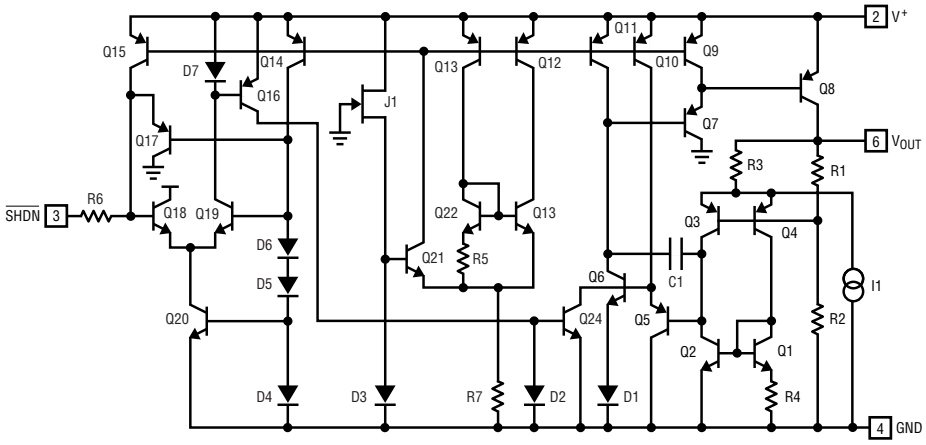

Figure 1. Simplified schematic of the LT1461

Table 1. LT1461 performance, $V_{IN} = V_{OUT} + 0.5V$

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	LT1461A	–0.04	——	0.04	%
	LT1461B	–0.06	——	0.06	
	LT1461C	–0.08	——	0.08	
	LT1461D	–0.15	——	0.15	
Output Voltage Temperature Coefficient	LT1461A	——	——	3	ppm/°C
	LT1461B	——	——	7	
	LT1461C	——	——	12	
	LT1461D –40°C to 125°C	——	——	20	
Load Regulation	Sourcing 0mA to 50mA	——	12	30	ppm/mA
Dropout Voltage	Sourcing 1mA	——	0.13	0.3	V
Supply Current	No Load	——	35	50	µA
Output Voltage Noise	0.1Hz ≤ f ≤ 10Hz	——	8	——	ppm_{P-P}
Long-Term Drift of Output Voltage	——	——	60	——	$ppm/\sqrt{kHr}$
Thermal Hysteresis	–40°C to 85°C	——	65	——	ppm

cause stress that is very different from stress that is caused by automatic testers at the LTC factory. Additionally, there is now an unrelieved mechanical bias on the leadframe when the solder cools. Figure 3 shows the SO-8 LT1461 output shift of about –100ppm after IR soldering onto a PC board. After 336 hours, as the stress relaxes, the output voltage typically shifts about 45ppm back toward the initial state where the device was factory trimmed.

Another type of stress is caused if a PC board is flexed, for example when held in a card cage. The stress on the board is transmitted directly to the IC package. A simply way to reduce the stress-related shifts is to mount the reference near the short edge of the PC board or in a corner. The board edge acts as a stress boundary, or a region where the flexure of the board is minimum. The package should be mounted so that the leads absorb the stress and not the package. (See "Understanding and Applying Voltage References," in *Linear Technology* VII:2 and VII:3, June and August, 1997, for more information on the effects of stress on voltage reference performance and techniques for mitigating it.)

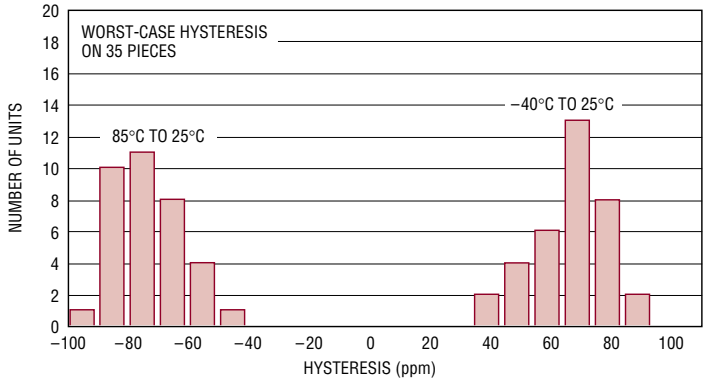

Figure 2. –40°C to 85°C hysteresis

Long-Term Drift

Some manufactures are now touting phenomenal long-term drift specifications. Long-term drift cannot be extrapolated from accelerated high temperature testing. This erroneous technique gives drift numbers that are wildly optimistic. The only way long-term drift can be measured is over the time interval of interest. The erroneous technique uses the Arrhenius Equation to derive an acceleration factor from elevated temperature readings. The equation is:

$$A_F = e^{\frac{E_A}{K} \cdot \left(\frac{1}{T1} - \frac{1}{T2}\right)}$$

where: E_A = Activation Energy (assume 0.7)

K = Boltzmann's Constant

T2 = Test Condition Temperature in Kelvin

T1 = Use Condition Temperature in Kelvin

To show how absurd this technique is, compare the LT1461 data. Typical 1000hr long-term drift at 30°C = 60ppm. The typical 1000hr long-term drift at 130°C = 120ppm. From the Arrhenius Equation the acceleration factor is:

$$A_F = e^{\frac{0.7}{0.0000863} \cdot \left(\frac{1}{303} - \frac{1}{403}\right)} = 767$$

The erroneous projected long-term drift is:

120ppm/767 = 0.156ppm/1000hr at 30°C

For a 2.5V reference, this corresponds to a 0.39µV shift after 1000 hr.

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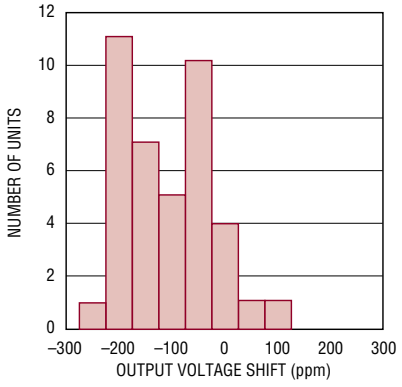

Figure 3. Typical distribution of output voltage shift after soldering onto PC board

Smart Battery Charger Is Programmed via the SMBus

by Mark Gurries

Introduction

Smart Batteries are becoming prevalent in the laptop computer world because they offer an industry-standard, high accuracy "gas gauge" system. These batteries conform to a set of specifications that define the operation of all of the components in a Smart Battery powered System (SBS). The battery has an embedded controller that tracks information related to battery charging and use. This information is provided to the system via a serial, 2-wire SMBus interface, a variant of the I²C™ bus in wide use today. The battery can be queried for information on remaining capacity, total capacity, time remaining at current rate of discharge, discharge current, terminal voltage and so on. Since most Smart Batteries can become a master on the bus, the battery can control the Smart Battery Charger for optimal charging. The LTC1759 Smart Battery Charger IC is designed to be controlled by this type of Smart Battery. In addition, a safety signal provided by the battery indicates whether the battery is present in the system and warns of possible thermal problems or battery faults if other systems fail. The emphasis of the SBS is on safety, ease of use and compatibility.

There are two types of Smart Battery Chargers (SBCs) allowed by the SBS specifications. A Level 2 charger, such as the LTC1759, is a slave on the SMBus and responds to commands from the battery to control charging. A Level 3 charger can be either a slave or a master on the SMBus, since it can query the battery to determine charging information. The SBC is independent of battery-chemistry type. It provides charging current and charging voltage in response to commands from the battery. Charge termination is sent by the battery as either zero current or zero voltage or as "terminate charge" alarm. Charging will also terminate if the safety signal indicates that the battery is not present or the battery is too hot to charge safely.

The LTC1759 is a complete Level 2 Smart Battery Charger. It is able to autonomously charge a Smart Battery by receiving and interpreting commands over its built-in SMBus interface. The LTC1759 adheres to all the safety requirements of the Smart Battery Charger Specification, including 3-minute timers that protect from SMBus communication failures and overcharging of Li-Ion batteries during wake-up mode—features absent from some competing solutions. Hardware-programmable current and voltage limits provide an additional level of protection that cannot be altered by errant software.

The LTC1759 manages all the complexities of a Smart Battery Charger System. This is appealing to those who wish to support Smart Batteries without getting involved in all the details. SBC compliance, safety, output voltage accuracy, SMBus accelerators and LTC's patented wall adapter current limiting are just a few of the features that make this an outstanding part.

LTC1759 Smart Battery Charger Features

The LTC1759 merges the intelligence of a Smart Battery Charger with a constant-current (CC), constant-voltage (CV), current mode switching battery charger circuit. The LTC1759 incorporates the following features:

- ❏ 0.5% output voltage accuracy at room temperature, 1% over temperature range
- ❏ 5% output current regulation
- ❏ An external, resistor-programmable voltage limit, with four ranges that support stacking of the popular 4.2V battery cell
- ❏ An SMBus programmable output voltage, from 2.465V to 21V in either 16mV or 32mV granularity, depending upon the programmed voltage range (10-bit resolution)
- ❏ An external, resistor-programmable current limit with four limits: 1A, 2A, 4A and 8A
- ❏ An SMBus programmable output current with 10-bit resolution over all ranges
- ❏ LTC's patented programmable AC wall adapter current limiting to maximize charge rate
- ❏ Low V_{IN}-to-V_{OUT} operation (dropout < 0.5V)
- ❏ 95% efficiency
- ❏ Compliant with Smart Battery Charger Specification Rev. 1.0, Level 2
- ❏ Low power consumption when AC is not present, while remaining compliant with all Smart Battery Charger requirements for status and interrupts
- ❏ Built-in SMBus accelerators (similar to the LTC1694)
- ❏ New 36-pin narrow SSOP package (0.209″ wide)

Circuit Description

The LTC1759 is composed of a synchronous, current mode, PWM step-down (buck) switcher controller, a charger controller, two 10-bit DACs to control charger parameters, a thermistor Safety Signal decoder, hardware voltage and current limit decoders and an SMBus controller block (refer to Figure 1).

The Smart Battery or system controller programs both constant-current (CC) and constant-voltage (CV) limit values though commands over the SMBus interface. The buck converter uses N-channel MOSFETs for switches, allowing low cost, high efficiency operation. It also provides reverse battery discharge protection and ultralow dropout operation. A

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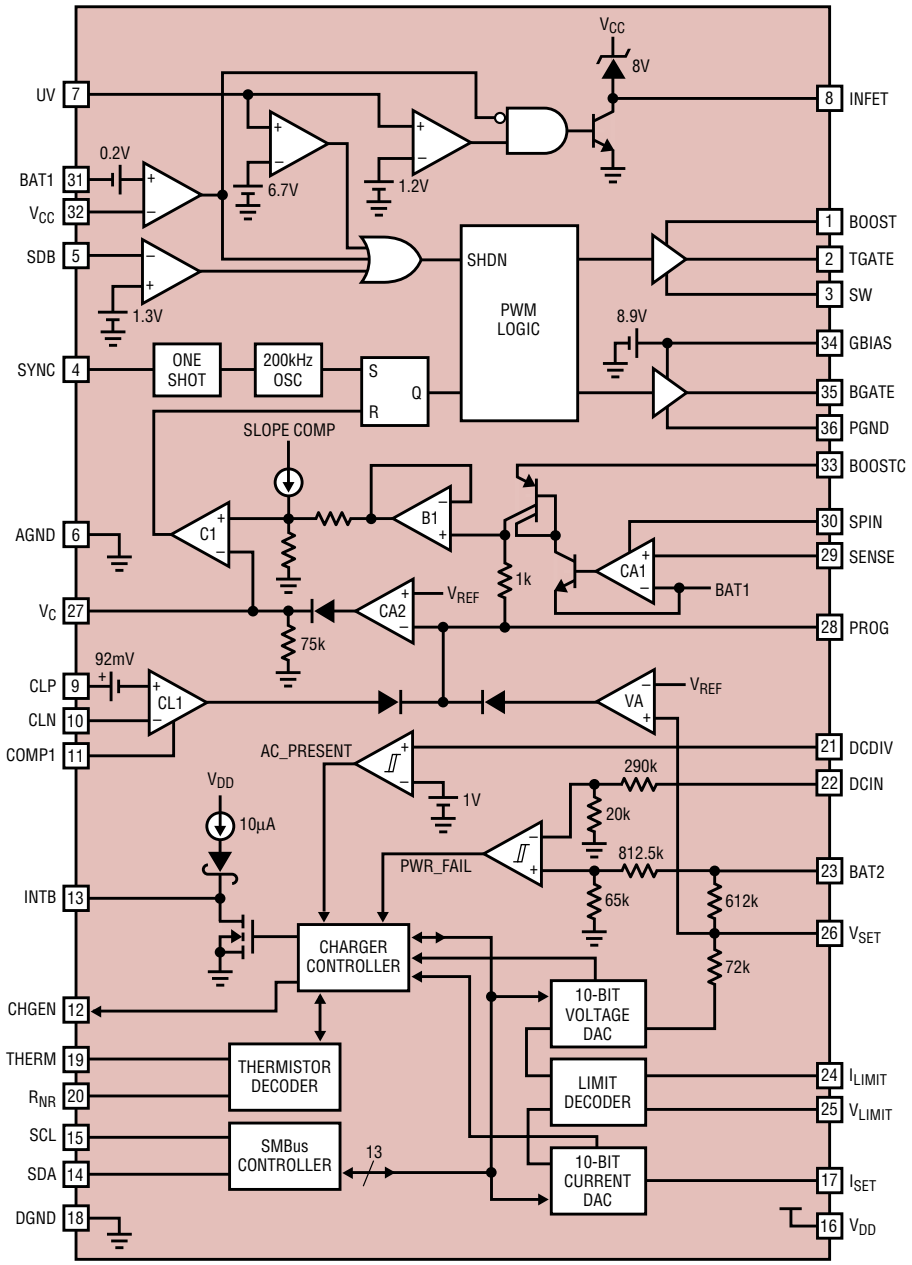

Figure 1. LTC1759 block diagram

thermistor safety-detection circuit isused to detect the presence of a battery and determine whether the temperature of the battery allows safe charging to occur. Linear Technology's patented input current limiting feature is implemented, allowing the fastest battery charge times without overloading the wall adapter.

When a constant current value is received via an SMBus transmission, it is scaled and limited to a value below that programmed by the R_{ILIMIT} resistor. This modified value programs the current DAC, setting the DC charging current. The current DAC is a 10-bit delta-sigma DAC that sinks current from the PROG pin when charging current is desired (refer to Figure 2). Amplifier CA1 senses the voltage drop across R_{SENSE} and forces this voltage across R_{S2} (200Ω); the current through R_{S2} is sent through a current mirror as a pull-up current on the PROG pin. The matching of current through R_{S2} with current from the PROG pin by CA2 implements constant-current operation. Since the delta-sigma DAC output is a series of pulses, a smoothing capacitor is needed to filter the pulses into DC.

When a constant-voltage value is received via an SMBus transmission, the value is scaled, adjusted to cancel offset and limited to a value below that programmed by the R_{VLIMIT} resistor. This modified value programs the voltage DAC, setting the DC charging voltage. The voltage DAC drives the bottom of an internal voltage divider network. The top of the voltage divider is connected directly to the battery output though the BAT2 pin. A voltage error amplifier, VA, compares the divided battery voltage on the V_{SET} pin with an internal, precision reference voltage. The output of the VA amp is configured as a current source that can drive the PROG pin. The PROG pin is a current summing node for both current and voltage feedback loops. The VA loop steals control of the current feedback loop when the battery voltage exceeds the programmed voltage, forcing the charging current down to the level required to maintain the programmed voltage. Since the ΔΣ DAC output is in the form of a series of pulses, a smoothing network is needed to filter the pulses into DC at the V_{SET} pin. The capacitors C5 and C4 form a capacitance divider that provides some filtering of the feedback voltage from the battery while filtering the DAC pulses.

The LTC1759 requires two power supplies. The PWM circuitry runs directly off the wall adapter supply through the V_{CC} pin, whereas the logic functions run independently from the V_{DD} supply. This allows the PWM circuitry to go into 40µA micropower shutdown mode when AC power is removed, allowing the logic and SMBus activity to remain alive, as required by Intel's ACPI standards. This separate supply also allows the logic and SMBus to run at 3V or 5V depending on the system designer's needs. To minimize power draw of the LTC1759 logic, the logic circuits are driven by a clock circuit that shuts down when there is no activity and wakes up to service SMBus activity or to generate interrupts. Once the request is serviced, the LTC1759 goes back to sleep.

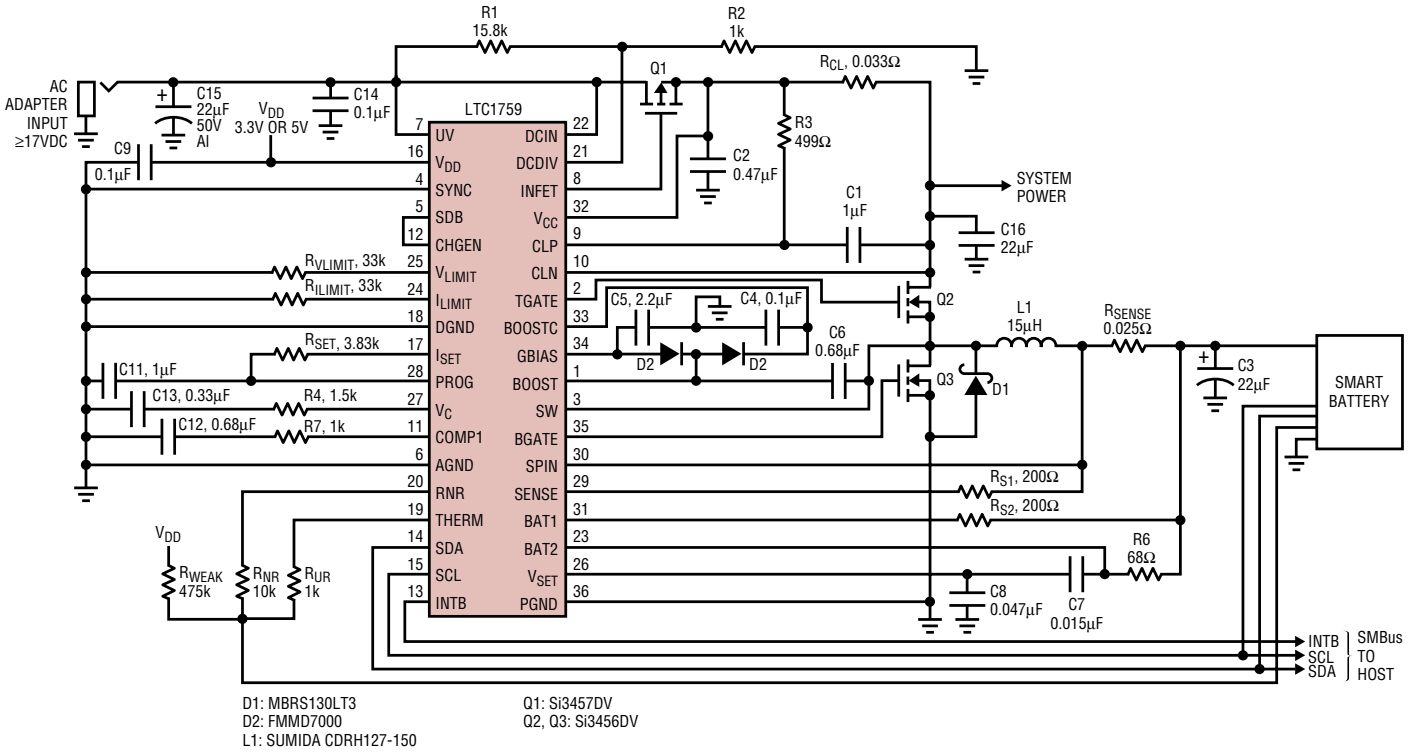

Figure 2. A complete 4A Smart Battery Charger

Shutdown of the PWM through the CHGEN–SDB pin combination occurs when the AC power is lost or the battery is removed. The LTC1759 detects the AC loss through the DCDIV pin. This threshold is usually set just below the lowest valid voltage of the wall adapter. AC power status may be read by the system over the SMBus. The UV pin is only used to put the PWM circuitry into micropower shutdown and is connected directly to the wall adapter supply.

Inductor selection is not critical with the design, since the loop response of the charger is intentionally set to be very slow. Almost any value will work, with a practical lower limit of about 15µH. Lower inductance will create higher ripple currents, requiring a lower ESR capacitor on the output. It will also cause cosmetically ugly discontinuous switching operation to occur at higher currents than necessary.

Output capacitor selection is not ESR critical but must be able to handle all of the ripple current from the charger. Do not count on the battery to carry the ripple current because the effective impedance as seen by the charger can be much greater than the ESR of the capacitor. Many battery packs have built-in series-protection MOSFETs that raise the ESR of the battery. There may also be optional power-routing MOSFETs in series with the battery in multiple-battery configurations, further increasing the battery ESR. From the charger point of view, the output capacitor ESR can be as high as 1Ω, allowing a wide range of capacitor options. When using a resistive or electronic load, some instability may occur. This can be fixed by adding a temporary 300Ω resistor in series with the PROG pin capacitor or putting a 10µF capacitor on the output. Avoid using ceramic capacitors in the output because they tend to make noise when the switcher goes discontinuous and starts to drop cycles at audible frequencies under very light load currents—use tantalums instead. Input capacitance selection is driven by the input ripple current of the charger, which is usually 1/2 of the maximum output current. For a 4A charger, a 22µF, 50V ceramic is recommended, since this part can typically handle 2A of ripple current. It also takes up the least amount of space and can cost less than other capacitor options.

Current protection, from battery to wall adapter, is provided by a P-channel MOSFET (Q1). A voltage comparator monitors the voltage across the MOSFET and will turn it off when the wall adapter drops to less than 200mV above the battery voltage. Although an inexpensive diode could be used instead of this MOSFET, the MOSFET only adds 100mV to the already low 0.4V dropout mode of operation without producing extra heat. During start-up without a battery, the MOSFET parasitic diode is used to allow wall adapter power to reach the V_{CC} pin and power up the PWM control circuitry.

Primary compensation is done on the PROG pin; however, DAC pulse filter requirements determine the effective value of the capacitor. Pulse ripple current must be less than 20mV or loop jitter will occur, giving the appearance of loop instability at light charging currents. The V_C pin capacitor's primary function is to provide soft-start support. There must always be a resistor of 1.5k in series

Table 1. I_{LIMIT} trip points and ranges

R_{ILIMIT}	Nominal Charging Current Range	Granularity
0Ω	0 < I < 1023mA	1mA
10k	0 < I < 2046mA	2mA
33k	0 < I < 4092mA	4mA
Open (>250k) or shorted to V_{DD}	0 < I < 8184mA	8mA

Table 2. V_{LIMIT} trip points and ranges

R_{VLIMIT}	Nominal Charging Voltage (V_{OUT}) Range	Granularity
0	2465 < V_{OUT} < 8432mV	16mV
10k	2465 < V_{OUT} < 12,640mV	16mV
33k	2465 < V_{OUT} < 16,864mV	32mV
100k	2465 < V_{OUT} < 21,056mV	32mV
Open or tied to V_{DD}	2465 < V_{OUT} < 32,768mV	32mV

with the V_C pin capacitor to allow proper shutdown.

From a thermal standpoint, the output voltage remains approximately 0.5% accurate over the battery temperature charging range. This higher precision allows a higher charge capacity in the battery, and, more importantly, will cause fewer problems with voltage-based charge termination circuitry in the battery.

SMB Alert

The SBS standards allow for the option of an open-collector interrupt line to notify the host when a critical power event has occurred. This feature is called SMBALERT#. The LTC1759 implements this feature by asserting the INTB line low when AC power is lost or restored and when a battery is physically installed or removed. INTB is cleared when the host reads the LTC1759 status register or performs a successful read of the SMBALERT# Response address of the LTC1759.

Setting Safe Voltage and Current Ranges

The LTC1759 voltage/current ranges are programmed with two external resistors, R_{VLIMIT} and R_{ILIMIT}, as shown in Tables 1 and 2. These limits prevent communication errors or errant software from causing the charger to damage the battery. At the same time, the variable granularity allows for better control of voltage and current in the lower ranges. The voltage limits are ROM mask programmable.

SMBus Acceleration

Unlike the I^2C bus, which allows the use of variable pull-up currents on the bus signals, the SMBus pull-up current is specified as a maximum of 350µA. In larger systems, the capacitance load on the SMBus can cause rise-time violations (T_{RISE} > 1µs), which could result in a communication failure. This is especially the case when I^2C devices are mixed with SMBus-compliant devices on the same bus. The thresholds of the I^2C bus receivers are generally higher than their SMBus cousins and are more sensitive to slow rise times.

Both SCL and SDA have dynamic pull-up circuits that improve the rise time on systems with significant capacitance on the two SMBus signals. The dynamic pull-up circuitry detects a rising edge on SDA or SCL and applies 2mA–5mA pull-up to V_{DD} for approximately 1µs (Figure 3). This action allows the bus to meet SMBus rise-time requirements with as much as 150pF on each SMBus signal. The improved rise time will benefit all of the devices that use the SMBus line, especially devices that use the I^2C logic levels.

AC Adapter Current Limiting

Wall adapters are typically AC/DC converters with 20V output at 3A–4A of load current. When a notebook is running, all of the available current from the wall adapter may be consumed by the system, leaving no power for charging the battery. However, as soon as the system's power requirements drop below the wall adapter's current limit, battery charging can resume. In order to recharge the battery in the shortest time possible, the recharging should start as soon as there is any current leftover from the system. The ideal situation is when the sum of battery charging current and the system current is just below the wall adapter's current limit. The LTC1759 incorporates a patented battery charger input current-limiting function that allows the charger current to be automatically

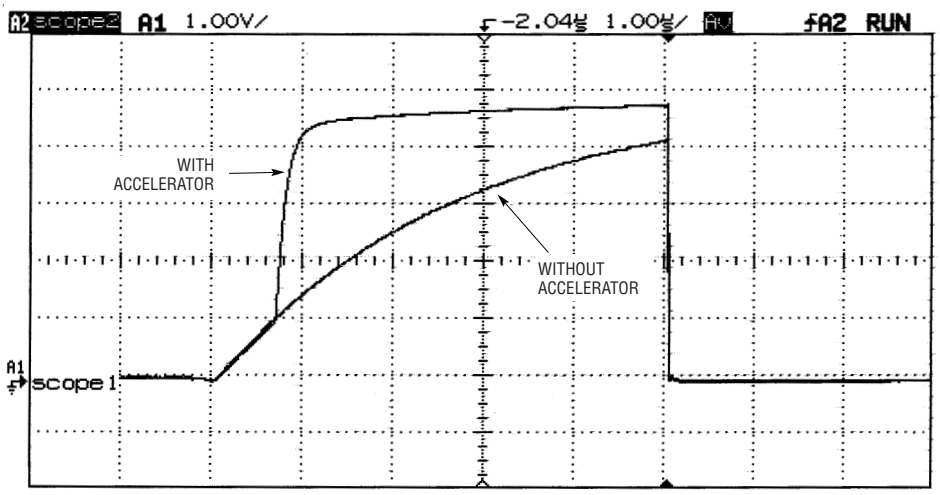

Figure 3. SMBus accelerator operation (R_{PULLUP} = 15k, C_L =150pF, V_{DD} = 5V)

Table 3. Safety signal resistance ranges

Safety Signal Resistance	ChargerStatus Bits	Description
0Ω–500Ω	SAFETY_UR = 1 SAFETY_HOT = 1 BATTERY_PRESENT = 1	Underrange
500Ω–3k	SAFETY_HOT = 1 BATTERY_PRESENT = 1	Hot
3k–30k	All Safety Bits Clear BATTERY_PRESENT = 1	Ideal
30k–100k	SAFETY_COLD = 1 BATTERY_PRESENT = 1	Cold
>100k	SAFETY_OR = 1 SAFETY_COLD = 1 BATTERY_PRESENT = 0	Overrange

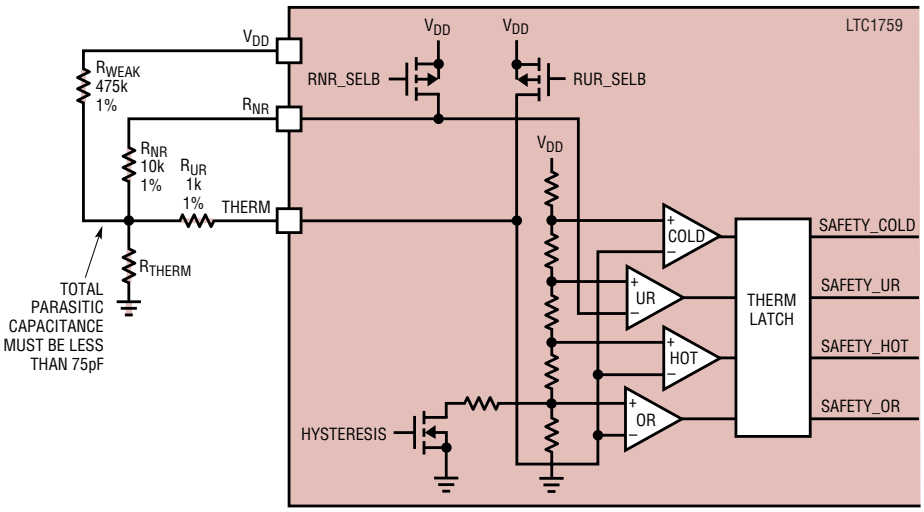

Figure 4. LTC1759 safety-signal-monitoring circuitry

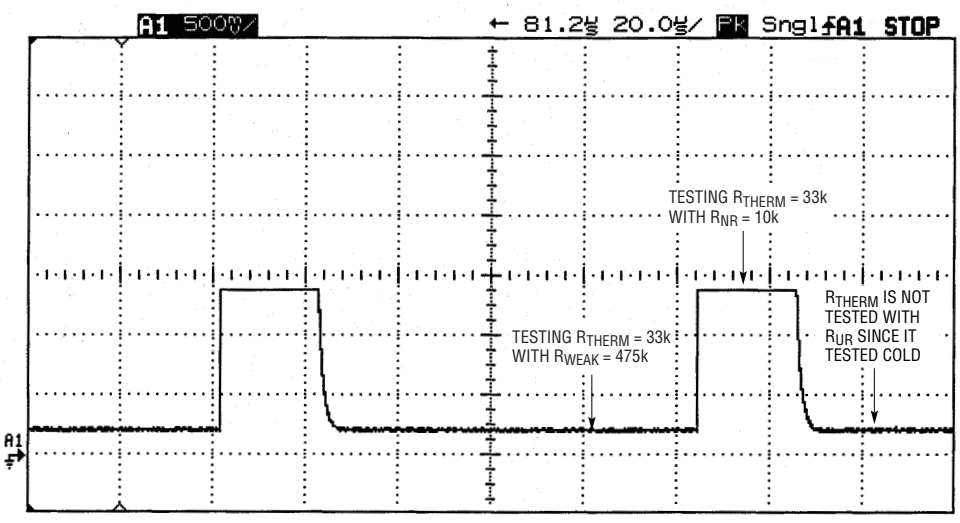

Figure 5. Testing a cold thermistor

reduced to avoid overloading the wall adapter, yet still charge the battery with the maximum available current.

Improved Safety Signal Sensing

The Safety Signal in most Smart Batteries is a resistor or thermistor to the battery's negative terminal. The SBC must sense the resistance of the Safety Signal to ground and determine if the battery is connected and whether it is safe to charge. The SBC must report the status of the Safety Signal during an SMBus read of the ChargerStatus() register. Table 3 shows the five ranges of resistance and what the ChargerStatus() bits must indicate.

The LTC1759 monitors the safety signal using a state machine to control the thermistor sensing scheme of Figure 4. This approach allows the LTC1759 to conserve power while supporting battery-presence detection and safety signal reporting when AC is not present. It also provides high noise immunity at the underrange-to-hot trip point.

The state machine sequentially switches R_{WEAK}, R_{NR} and R_{UR} to pull-up against the battery's internal thermistor. The resulting voltage is monitored by the comparators and used to determine the thermistor's operating range. The state machine is able to sample the safety signal with all three resistors in 100µs. This allows the thermistor to be read during an SMBus read requesting Safety Signal status and then shut down to conserve power. A system using a fixed 10k pullup for all ranges will waste current when AC is not present. R_{WEAK} is used to continuously monitor battery presence; it uses very little current and allows detection of the insertion or removal of a battery regardless of whether or not AC is present. R_{NR} is used to determine if the safety range is cold or ideal. R_{UR} is used to determine if the safety range is hot or underrange. The testing of R_{THERM} is shown for a cold and underrange thermistor in Figures 5 and 6, respectively. When AC is present, the state machine continuously tests the

continued on page 18

LTC1755 Smart Card Interface Provides Inductorless Boost and Signal-Level Translators

by Steven Martin

Introduction

Already common in Europe and some of the Far East, smart cards may soon replace magnetic stripe cards in the U.S. The LTC1755 provides a simple and complete solution to smart card interfacing. Requiring only two bypass capacitors and one charge pump capacitor, the LTC1755 interfaces seamlessly between a smart card socket and a host microcontroller. It is designed to comply with all of the available electrical standards for smart card interfacing. Figure 1 shows the LTC1755 in a typical smart card application.

Figure 2 shows the block diagram of the LTC1755. An internal power management unit delivers a selectable 3V or 5V regulated output voltage to the smart card. Two unidirectional and three bidirectional communication channels provide the signal translation necessary to interface from a microcontroller at one supply voltage to a smart card at another supply voltage. A smart card detection channel observes the state of a mechanical switch and delivers the information to the microcontroller after an appropriate debounce period. Finally, the LTC1755 provides all fault detection necessary to comply with both the EMV and ISO-7816-3 smart card standards. These include short-circuit detection, smart card removal during a transaction and undervoltage and overtemperature faults. In the event of a fault condition, the smart card is properly deactivated and an alarm output notifies the microcontroller of the fault.

Power Management Unit

Unlike solutions that require an external inductor and current sense resistor to generate power to the card, the power management section of the LTC1755 requires only a small flying capacitor to provide step-up capability. Sense circuitry determines how much input voltage is available and decides whether to step the input voltage up or down to provide the required output voltage to the smart card. For example, if the input supply voltage is 3.3V and the required smart card voltage is 5V, the LTC1755 will operate as a charge pump to deliver the higher voltage; if the input supply voltage is 5V and the required smart card voltage is 3V, it will automatically step down to provide the correct output voltage.

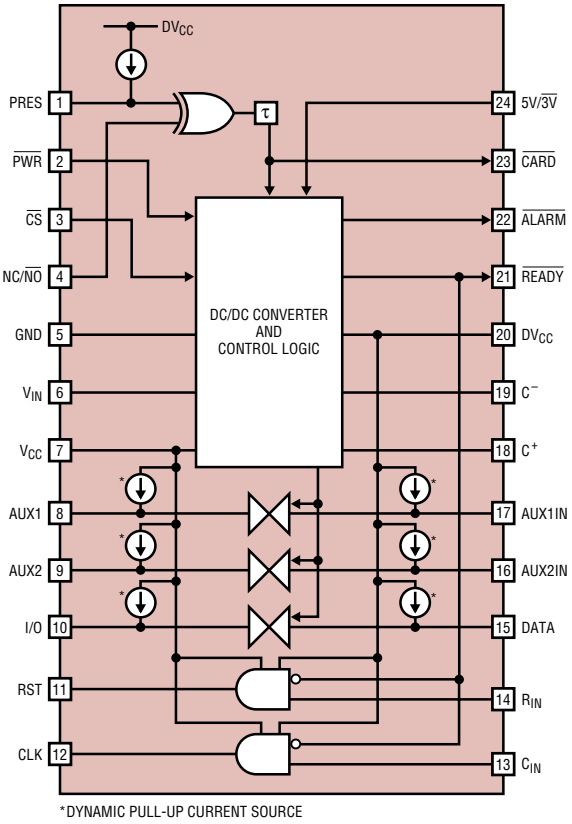

Figure 2. LTC1755 block diagram

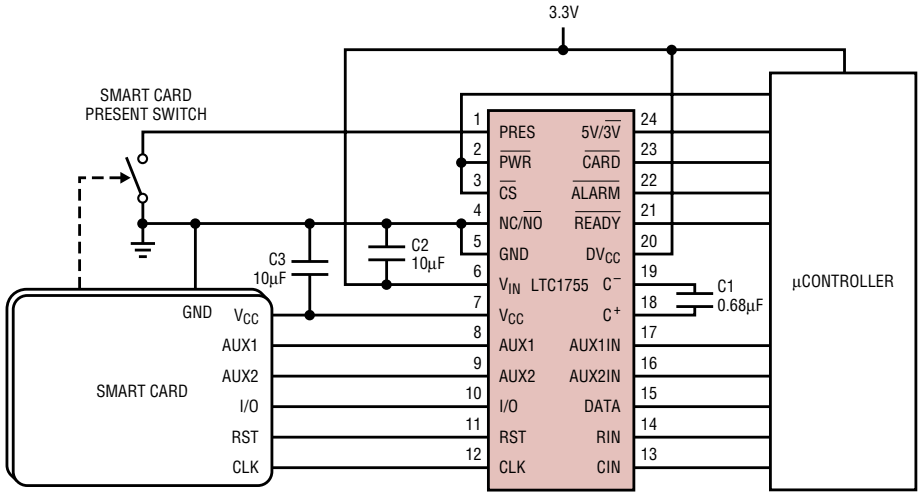

Figure 1. LTC1755 typical application

The entire LTC1755, including the power management circuitry, is designed to consume low power under light or no load conditions. This can result in considerable power savings for battery-powered applications. Furthermore, the shutdown current is only several microamperes.

To prevent high inrush current during turn-on, an automatic soft-start feature increases the supply voltage of the smart card at a fixed rate. This is particularly important when the LTC1755 is in step-up mode because the input current will be twice the output current. With a 10µF output capacitor, the rise time of approximately 2ms limits the input current to 50mA, thus preventing start-up problems. The $\overline{\text{READY}}$ pin tells the microcontroller when the output voltage has reached its final value. This signal also enables the communication channels, thereby ensuring proper compliance with smart card standards. Figure 3 shows the card supply voltage ramp as well as the $\overline{\text{READY}}$ pin indicating that the output has reached its final state.

During smart card deactivation, either by direct user control or by automatic fault deactivation, the LTC1755 discharges the smart card supply pin in under 250µs. Rapid discharge is important to ensure that the card's supply is completely removed in the event of smart card removal during a transaction. This requirement is specified in various smart card standards.

Bidirectional Communication Channels

There are three bidirectional channels for communicating with the smart card. These channels, which are open-drain I²C™ style, provide level translation, direction arbitration and short-circuit protection. Unlike analog approaches, the LTC1755 uses control logic with active pull-up and pull-down devices on both sides of the channel. This allows the required source and sink currents to be achieved independent of the input voltage on the transmitting side of the channel. The direction-control logic arbitrates which side of the channel is the *talker* and which side is the *listener*. Upon receipt of a low on one side of the channel, that side becomes the talker and the other side becomes the listener. Transmission in the opposite direction is instantly blocked to prevent the channel from latching. Once the talker side of the channel is relinquished, both sides return high and either side is a candidate to become the next talker.

To meet the stringent rise-time requirements imposed by ISO-7816-3 while keeping power dissipation and V_{OL} to a minimum, an accelerator circuit (see Figure 4) is built into each pull-up current source on the bidirectional channels. Normally, a small current, I_{START}, pulls each bidirectional pin to its respective power supply rail. An open-drain transistor can easily overcome I_{START} whenever a low is asserted. When the low is relinquished, I_{START} slowly begins to charge the pin toward its rail again. An internal edge-rate-detection comparator notices that the node is moving upward and fires a large pull-up current source to assist. Once the larger current source begins to enhance the edge rate of the node, the decision to enhance is reinforced, thereby effecting a dynamic form of hysteresis. After the node has reached the power supply rail, the comparator resets and only I_{START} is available again. Figure 5 shows the waveform of a bidirectional pin. The 10% to 90% rise time is on the order of 150ns.

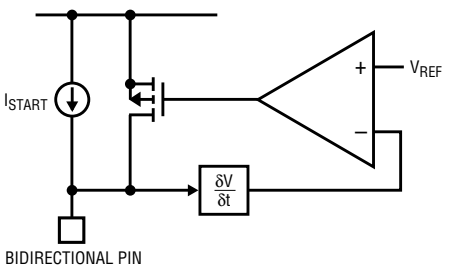

Figure 4. Dynamic pull-up current source

Unidirectional Communication Channels

There are two unidirectional channels on the LTC1755 that provide the level-shifted clock and reset signals used by the smart card for synchronization. The clock channel is designed specifically for high speed and can faithfully transmit a 5MHz signal. Both of these channels are disabled and provide a valid low before the smart card supply voltage has reached its final value. Once the card supply voltage is valid, these channels will simply transmit the signals present

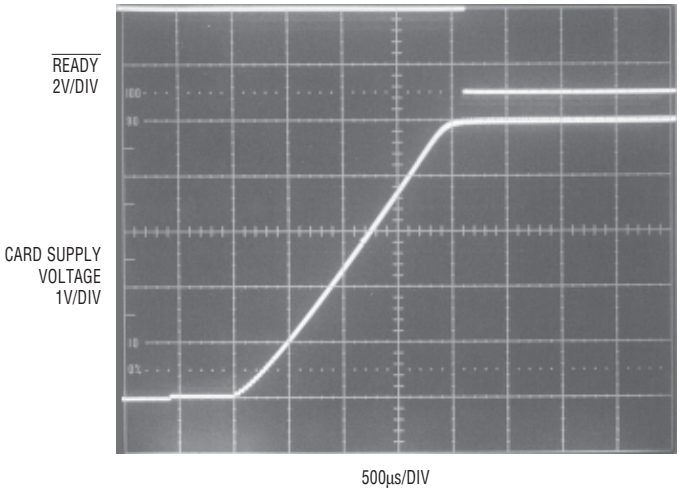

Figure 3. Smart card supply voltage and $\overline{\text{READY}}$ upon activation

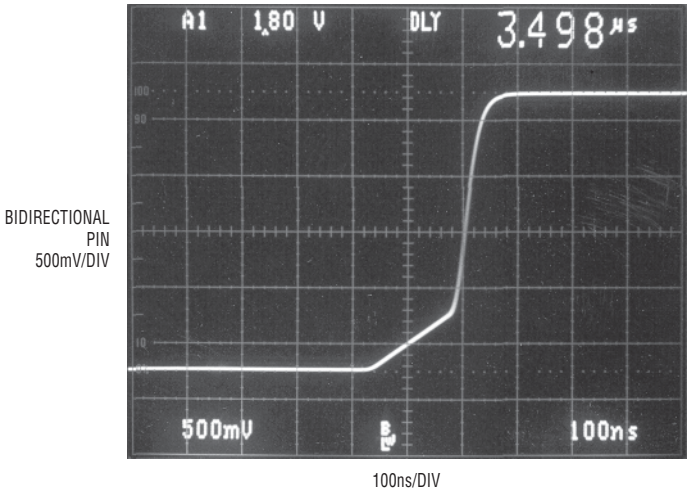

Figure 5. Bidirectional pin with dynamic pull-up

at their respective inputs. To comply with smart card standards, the RST pin is always brought low before the CLK pin upon deactivation.

Smart Card Detection Channel

The LTC1755 incorporates the only card detection solution that does not require additional de-bounce circuitry or software. This channel detects the presence of a smart card by forcing a small current and monitoring the voltage on a mechanical detection switch. Once a smart card is detected, the channel starts the debounce timer. The presence of a card is reported to the microcontroller only if the card has been present for a minimum of 40ms. Existing solutions provide either no debounce capability or minimal (only tens of microseconds) debounce time. These solutions require additional software or hardware to mask out the transients associated with the physical insertion of the smart card. Also, unlike other solutions, the switch-sense current is generated by the LTC1755 so no external components are required. Once a valid card indication occurs, the channel alerts the microcontroller by asserting the $\overline{\text{CARD}}$ pin.

For maximum flexibility the smart card detection channel can be programmed to respond to either a normally open or normally closed switch. A built-in XOR gate is used as a controlled inverter to provide this function.

Fault Detection and Avoidance

Specifications relating to faults on the smart card pins are very stringent. For example, ISO7816-3 (section 1.4.8) specifies that the smart card socket must be capable of surviving a "metal plate" connection between any or all contacts without damage. To accommodate these fault conditions, the LTC1755 uses voltage sensing on the low impedance pins to detect if they are being forced to an inappropriate level. For example, the voltage on the smart card supply pin, V_{CC}, is compared with an internal reference to determine if a short circuit exists. If a fault persists for a prescribed period, the LTC1755 automatically deactivates the smart card and asserts the $\overline{\text{ALARM}}$ output. The small timeout period prevents false errors from plaguing the microcontroller. The clock and reset channels respond to faults in a similar way. The digital levels on the outputs of these channels (CLK and RST) are compared to those being presented at their inputs. If these signals differ for several microseconds, a fault is declared and the smart card is deactivated. Again, the $\overline{\text{ALARM}}$ output alerts the microcontroller that an electrical fault exists. In both cases, since the smart card becomes deactivated, there is no power available to deliver excessive current for a prolonged period.

The three bidirectional pins on the smart card side of the channel are protected against short circuits to the smart card supply voltage by means of a constant-current pull-down output. Rather than a simple pull-down transistor to transmit a low to the smart card, these channels use a current source implementation. The 3.5mA current source provides enough current to meet the edge rate and V_{OL} requirements while limiting the current available during a fault. The available smart card standards specify that no more than 5mA flow during faults on these pins. Of course, short circuits to ground on these channels are indistinguishable from a normal signal and must be detected by the data-error checking routines.

Conclusion

The LTC1755, designed specifically for smart card applications, provides all of the necessary level shifting and power circuitry to interface with a smart card socket. To further reduce board level complexity, it includes a smart card detection channel with built-in debounce circuitry. Since the LTC1755 provides all of the necessary smart card interface functions, only bypass capacitors and one charge pump capacitor are required for operation. Under most circumstances the operation of the LTC1755 is simple and provides a nearly transparent path to the smart card. However, when an electrical error condition occurs the LTC1755 responds quickly by powering down the smart card and alerting the microcontroller.

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LT1306: Synchronous Boost DC/DC Converter Disconnects Output in Shutdown

by Bing Fong Ma

Introduction

Step-up or boost DC/DC converters traditionally suffer from a lack of true shutdown capability. The output of a boost converter is connected to the input through the inductor and diode; when the device is powered down, the load is still connected to the input source, presenting a possible discharge path. Even some synchronous boost converters suffer from this limitation. The unique configuration of the LT1306's internal 2 ampere switch and rectifier overcomes this limitation. When the LT1306 is shut down, the output is disconnected from the input, eliminating the discharge path.

Additionally, the LT1306 can regulate the output when the input voltage exceeds the output voltage. This is useful for generating a 5V supply from a 4-cell alkaline battery. When fresh, the battery voltage measures about 6.5V, but when depleted, the battery voltage is only 4V. A simple boost converter output will follow the input voltage only when the battery voltage exceeds 5V, while a step-down, or buck converter will lose regulation when the battery voltage falls below 5V. The LT1306 regulates the output to 5V in both situations.

Lastly, the LT1306 controls inrush current. A user installing a new battery need not worry about high inrush current as the battery initially charges the output capacitor. The LT1306 provides a clean solution to a difficult problem.

The LT1306 packs all these features in an SO-8 package. The constant frequency, current mode PWM device runs at 340kHz and features Burst Mode™ operation to maintain high efficiency at light loads. No-load quiescent current is 160µA, while the device consumes just 9µA in shutdown. The device can be externally synchronized to frequencies between 425kHz and 500kHz.

Circuit Description

In the block diagram of Figure 1, the PWM control path is shown enclosed within the dashed line. The free-running frequency of the oscillator is trimmed to 340kHz. The main power switch, Q1, is turned on at the trailing edge of the clock pulse. Q1 is switched off when the switch current (sensed across resistor R_S) exceeds a

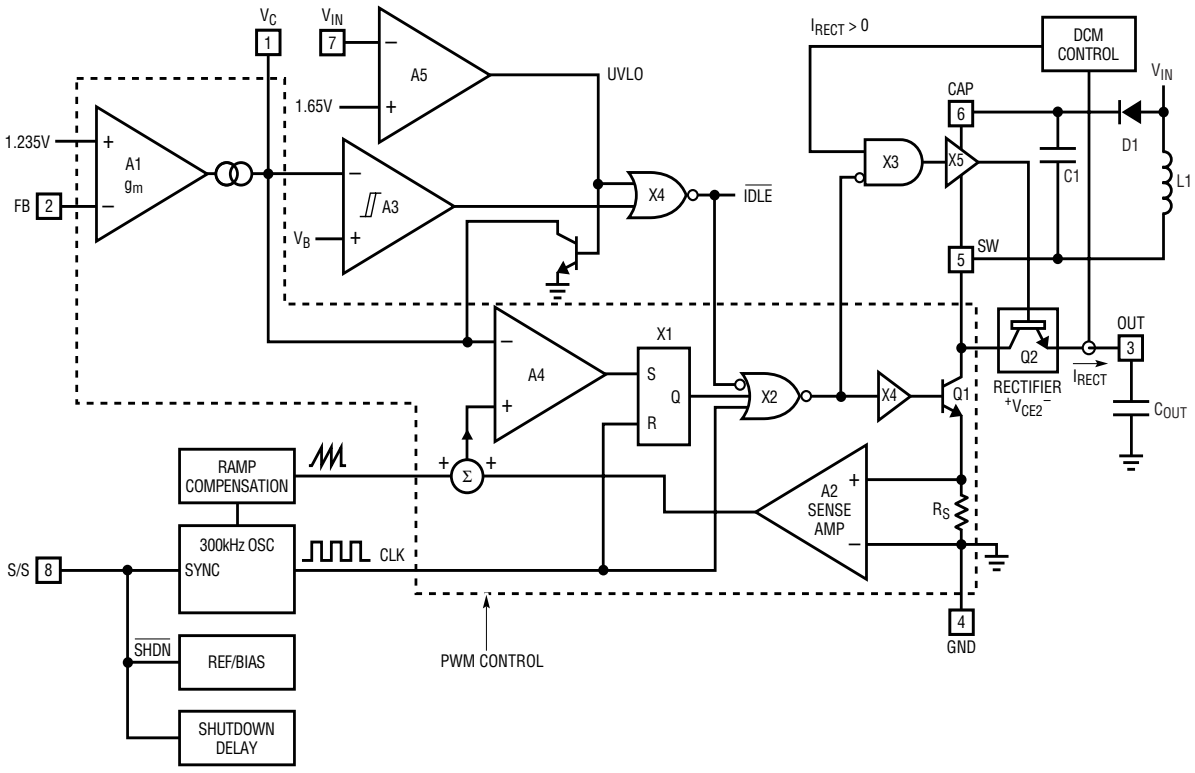

Figure 1. LT1306 block diagram

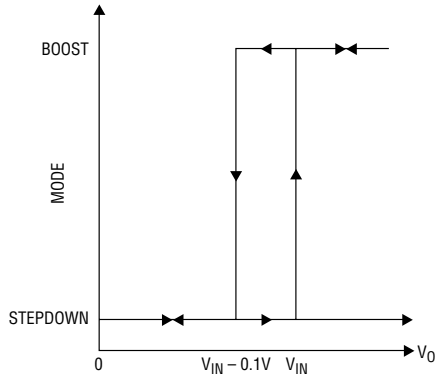

Figure 2. DC transfer characteristics of the mode control comparator plotted with V_O as an independent variable; V_{IN} is considered fixed.

programmed level set by the error amplifier output, V_C, and the compensation ramp. This is current mode control. The switch current limit is reached when V_C clamps at 1.28V.

The error amplifier output determines the peak switch current required to regulate the output voltage. V_C is therefore a measure of the output power. At heavy loads, the peak and average inductor current are both high. The LT1306 operates in continuous-conduction mode (CCM) as V_C increases. As the load decreases, the average inductor current moves lower with an accompanying decrease in the peak inductor current. If the inductor current returns to zero within each switching cycle, the converter is said to operate in discontinuous-conduction mode (DCM). Further reduction in load moves V_C towards its lower operating range.

Hysteretic comparator A3 determines if V_C is too low for the LT1306 to operate efficiently. As V_C falls below the Burst Mode threshold, V_B, comparator A3 turns off Q1. Any energy stored in the inductor is delivered to the output through the synchronous rectifier. The LT1306 draws only 160µA from the input in this idle state. As the output voltage droops, V_C rises above the upper trip point of A3. The LT1306 again wakes up and delivers power to the load. If the load remains light, the output voltage will rise and V_C will fall, causing the converter to idle again. Power delivery therefore occurs in bursts. The burst frequency is dependent on the input voltage, the inductance, the load current and the output filter capacitance. The output voltage ripple in Burst Mode operation is higher than those in CCM and DCM operation. Burst operation increases light load efficiency because the higher peak switch current characteristic of Burst Mode operation allows the converter to deliver more energy in each switching cycle than possible with cycle-skipping DCM operation. Thus, fewer switching cycles are required to maintain a given output. Chip supply current also becomes a small fraction of the total input current.

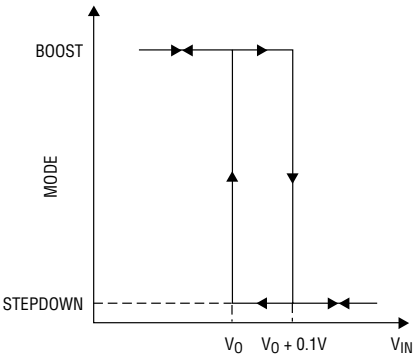

Figure 3. DC transfer characteristics of the mode control comparator plotted with V_{IN} as an independent variable; V_O is considered fixed.

The synchronous rectifier is represented as an NPN transistor, Q2, in the block diagram. A rectifier driver, X5, supplies variable base drive to Q2 and controls the voltage across the rectifier. The supply voltage for driver X5 is generated locally with the bootstrap circuit comprising D1 and C1. When switch Q1 is on, the bootstrap capacitor C1 is charged from the input to the voltage $V_{IN} - V_{D1(ON)} - V_{CESAT1}$. The charging current flows from the input through D1, C1 and Q1 to ground. After Q1 is switched off, the node SW goes above V_O by the collector–emitter saturation voltage of Q2. D1 becomes reverse biased and the CAP pin voltage is approximately $V_O + V_{IN} - V_{D1(ON)}$. The capacitor C1 supplies the Q2 base drive. The charge consumed is replenished during Q1's on-interval.

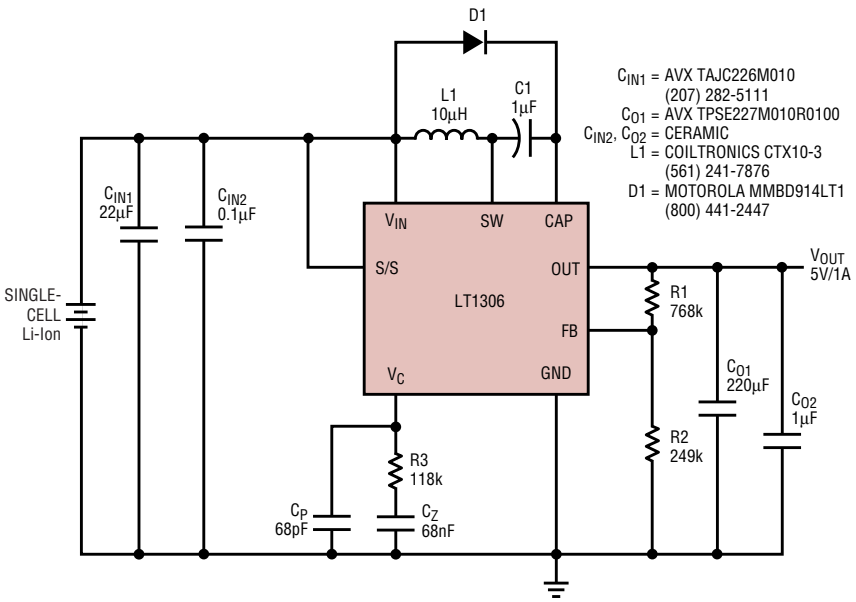

Figure 4. Single Li-Ion cell to 5V converter

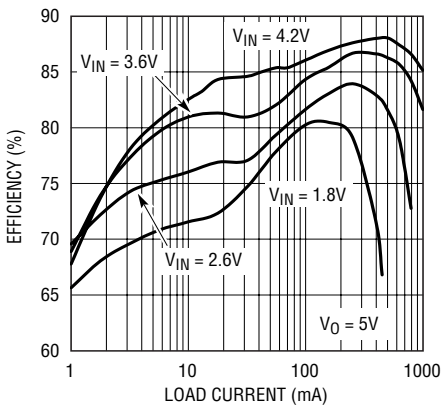

Figure 5. Efficiency of Figure 4's circuit

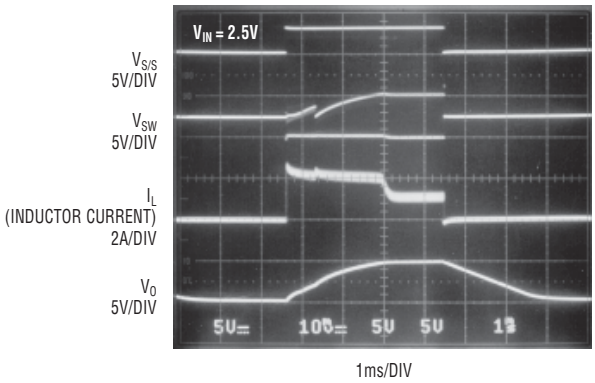

Figure 6. Start-up to shutdown transient response: note that the input start-up current is well controlled and that the output falls to zero in shutdown (I_L is also the input current, as the inductor is at the input).

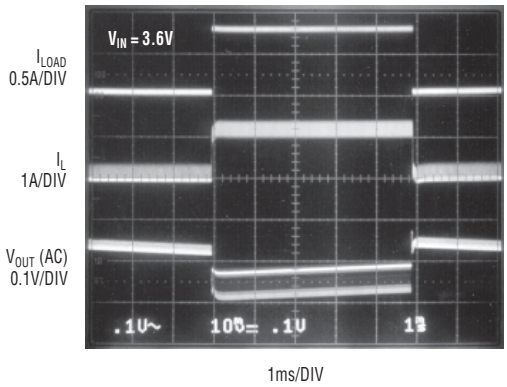

Figure 7. Transient response of the converter in Figure 4 with a 50mA to 800mA load step

In boost operation, X5 drives the rectifier Q2 into saturation with constant forced β. X5 ceases supplying base current to Q2 when the inductor current falls to zero. If V_{IN} is greater than V_O, Q2 will not be driven into saturation. Instead, the collector–emitter voltage of Q2 increases so that the inductor voltage reverses polarity as Q1 switches. Since the inductor voltage is always bipolar, volt-second balance can be maintained regardless of the input voltage. The LT1306 can therefore operate as a step-down converter.

During start-up, the inductor voltage of a boost converter with a diode rectifier remains positive until the output voltage rises to one diode voltage below the input voltage. A high input-transient current spike invariably results. In the LT1306, the inductor voltage reverses polarity every switching cycle. This, with cycle-by-cycle current limit, eliminates the inrush current spike.

The rectifier voltage drop depends on both the input and output voltages. Efficiency in step-down operation is approximately that of a linear regulator. For sustained step-down operation, the maximum output current will be limited by the package thermal characteristics.

A hysteretic comparator inside driver X5, which detects the crossover between the input and the output voltages, signals the driver to provide appropriate base current to the rectifier. DC transfer characteristics of this comparator are illustrated in Figures 2 and 3.

When shutdown is activated ($V_{S/S}$ < 0.45V), all circuits except synchronous rectifier Q2 and its driver X5 are shut off. If V_O is above V_{IN}, Q2 will be driven into saturation. Stored inductive energy flows to the output through the saturated rectifier. As V_O falls below V_{IN}, X5 reduces the base drive to Q2, which increases the rectifier voltage. The inductor voltage is now negative. The inductor current continues to fall to zero. The driver X5 then turns off and the rectifier Q2 becomes an open circuit. The LT1306 consumes 9µA from the input in shutdown.

Single Li-ion Cell to 5V Converter

The LT1306 is ideally suited for generating 5V output from a single Li-ion cell. The circuit shown in Figure 4 is capable of supplying 1A of DC output current. The value of resistor R3 is chosen so that the overall feedback loop gain crosses 0dB before the right-half plane (RHP) zero. The capacitor C_Z and the resistor R3 form a low frequency zero in the loop response. C_P ensures adequate gain margin beyond the RHP zero. The value of R3 is inversely proportional to the error amplifier g_m. Low g_m and high R3 improve converter load-transient response.

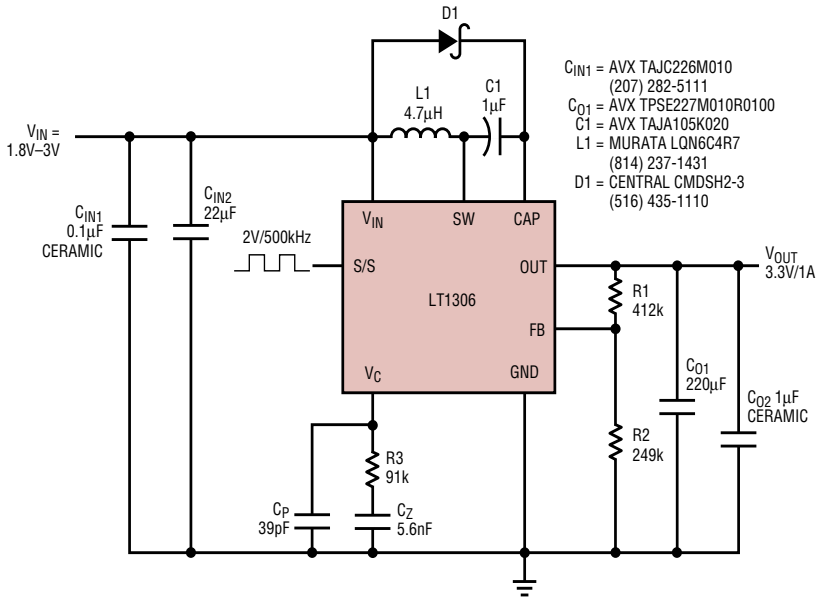

Figure 8. 2-cell to 3.3V output converter

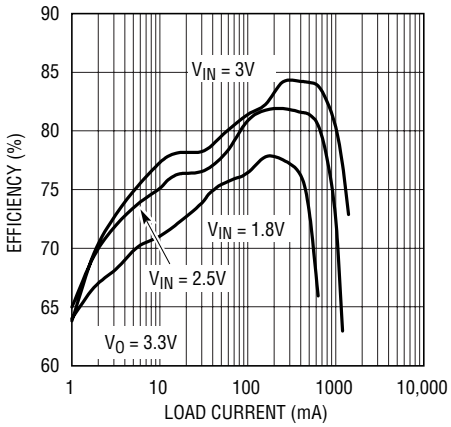

Figure 9. Efficiency of Figure 8's circuit

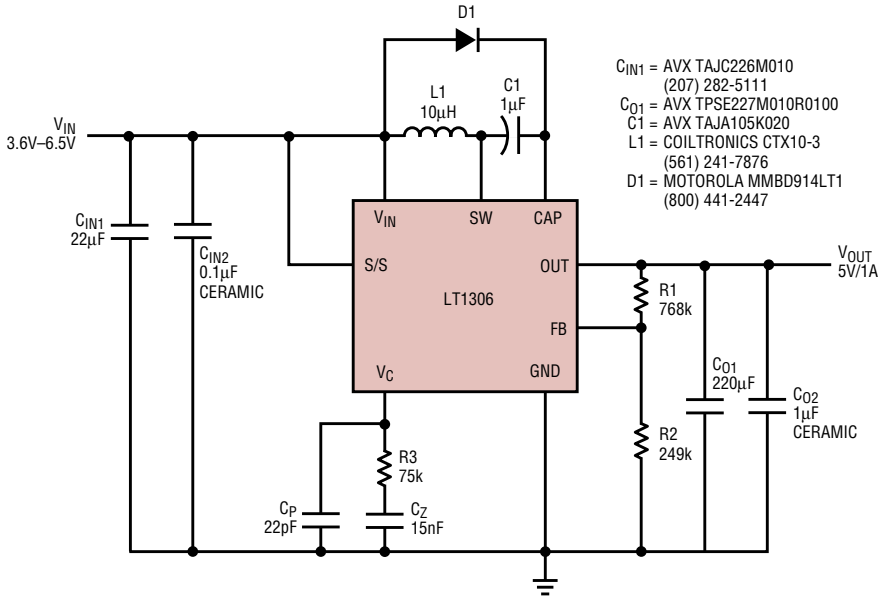

Figure 10. 4-cell to 5V output converter

In applications where high pulse current (>1A) is drawn from the output, a large electrolytic capacitor (>1000µF) is typically used to hold up the output voltage during the load pulse. Higher output filter capacitance lowers the dominant pole frequency of the gain response so that higher loop gain (that is, a higher value of R3) is required in the compensation network to give the same loop crossover frequency.

Efficiency curves of the converter are shown in Figure 5. Figure 6 shows a start-up-to-shutdown transient. The converter operates in step-down mode until the output voltage exceeds the input voltage (2.5V). The mode switching is evidenced by the sudden decrease in the SW node voltage. The input start-up current is well controlled at the switch current limit of 2.2A. The converter then produces a steady state output of 5V. Pulling the S/S pin low for at least 33µs disconnects the load. Figure 7 shows the load transient response of the converter.

2-Cell to 3.3V Converter

Figure 8 depicts an externally synchronized 2-cell to 3.3V converter running at 500kHz. A 4.7µH inductor is used to take advantage of the higher switching frequency. Driving the S/S pin with a clock generator, which has a 2V amplitude and less than 20ns of rise time, synchronizes the LT1306. Synchronization is positive-edge triggered. Diode D1 is a CMDSH2-3 Schottky diode. Compared to a junction diode, a Schottky diode increases the bootstrap voltage and affords higher operating headroom for rectifier Q2. In situations where reduced headroom is acceptable (such as over the commercial temperature range), a 1N4148 or 1N914 diode can also be used. The converter efficiency is plotted in Figure 9.

4-Cell to 5V Converter

Due to its ability to establish volt-second balance with V_{IN} greater than V_O, the LT1306 is also suited for applications where the battery voltage straddles the desired output voltage. One such example is the 4-cell to 5V converter shown in Figure 10.

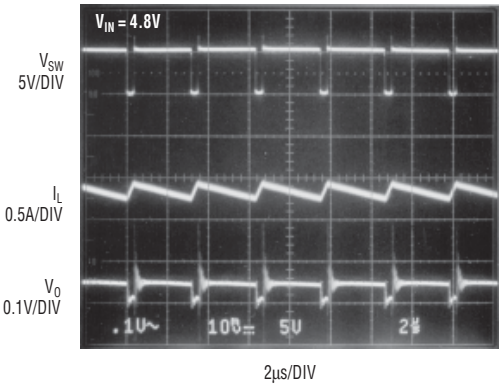

Figure 11. Continuous conduction mode switching waveforms in boost mode; V_{IN} = 4.8V, V_O = 5V

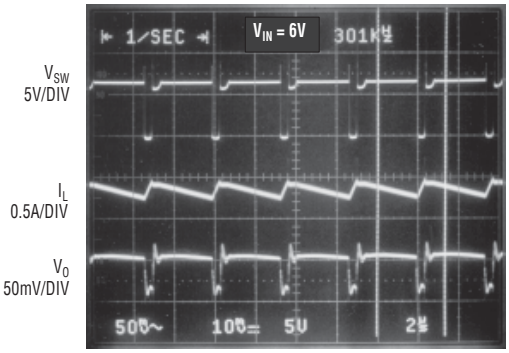

Figure 12. Continuous conduction mode switching waveforms in step-down mode; V_{IN} = 6V, V_O= 5V

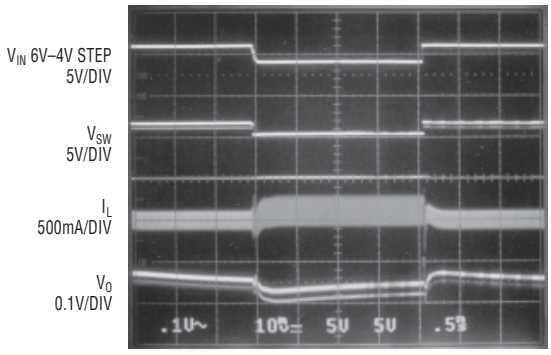

Figure 13. Transient response of the circuit in Figure 10 with step input (4V–6V)

The continuous-conduction mode switch-node voltage and the inductor current for step-down operations (Figure 12) are contrasted with those of boost operation in Figure 11. Note that in step-down mode, when the rectifier is conducting, the switch voltage exceeds V_{IN}. Input step (from 4V to 6V) transient response is illustrated in Figure 13. The converter efficiency is plotted in Figure 14.

Conclusion

The LT1306 is a complete synchronous boost DC/DC converter offering a set of features that few competing devices are able to match. The unique rectifier design results in a boost/step-down converter that disconnects the load in shutdown and controls input current during startup.

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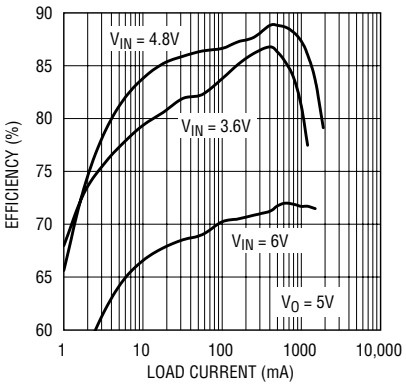

Figure 14. Efficiency of Figure 10's circuit

Smart Battery, continued from page 10

thermistor every 100µs. When AC is not present, R_{NR} and R_{UR} thermistor testing occurs only when a battery is first inserted or removed or during a transmission requesting Safety Signal status.

The underrange detection scheme is a very important feature of the LTC1759. As can be seen from Figure 6, the R_{UR}/R_{THERM} trip point of 0.333 • V_{DD} (1V) is well above the 0.047 • V_{DD} (140mV) threshold of a system using a 10k pull-up for all ranges. A system using a 10k pull-up would not be able to resolve the important underrange-to-hot transition point with a modest 100mV of ground offset between the battery and thermistor-detection circuitry. Such offsets are anticipated when charging at normal current levels.

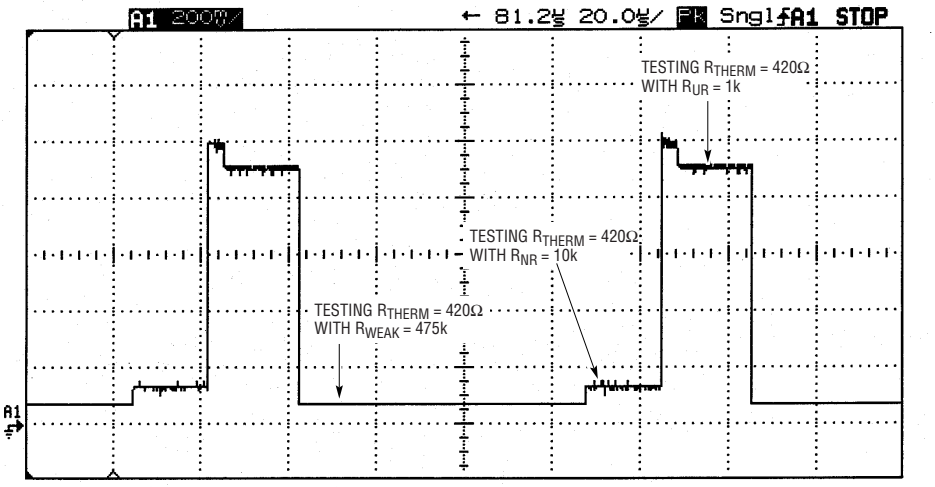

Figure 6. Testing an underrange thermistor

Conclusion

The LTC1759 complies with the Smart Battery Charger standard published by the Smart Battery System organization, in which Linear Technology is a promoter and voting member. The charger controller also complies with Intel's ACPI standard by being able to respond to system commands even when there is not AC wall adapter power. The charger offers the widest current and voltage range of operation compared to competitive parts. Feature for feature, it also offers the highest integration possible today with a Smart Battery Charger. The LTC1759 achieves significant cost savings, performance and safety advantages over other Smart Battery Chargers currently available.

Versatile Dual Hot Swap Controller/ Power Sequencer Allows Live Backplane Insertion

by Bill Poucher

Introduction

When a circuit board is inserted into a live backplane, the supply bypass capacitors on the board can draw large transient currents from the backplane power bus as they charge. These transient currents can destroy capacitors, connector pins and board traces and can disrupt the system supply, causing other boards in the system to reset. The new dual-channel LTC1645 Hot Swap controller is designed to ramp a circuit board's supply voltages in a controlled manner, preventing glitches on the system supply and damage to the board.

The LTC1645's two channels can be set to ramp up and down separately, or they can be programmed to rise and fall simultaneously, ensuring power supply tracking at the two outputs. Using external N-channel pass transistors, the supply voltages can be ramped at a programmable rate. Two high-side switch drivers control the external N-channel FET gates for supply voltages ranging from 1.2V to 12V. Programmable electronic circuit breakers protect against shorts at either output. The LTC1645 is available in the 14-pin and 8-pin SO packages. The 14-pin version additionally provides a system reset signal and a second "spare" comparator to indicate when board supply voltages drop below user-programmable levels. It also has a fault signal to indicate an overcurrent condition and a timer pin to create a delay before ramping up the supply voltages and deasserting the system reset signal.

Typical Hot Swap Application

Figure 1 shows a typical Hot Swap application using the LTC1645. Q1 and Q2 control the board's power supplies, R_{SENSE1} and R_{SENSE2} provide current fault detection and R1 and R2 prevent high frequency oscillation. By ramping the gates of the pass transistors up and down at a controlled rate, the transient surge current (I = C • dv/dt) drawn from the main backplane supply is limited to a safe value when the board makes connection.

The timing for the board is shown in Figure 2. When power is first applied to the chip, the gates of the FETs (GATE1 and GATE2 pins) are pulled low. Once the ON pin rises at time point 1, the LTC1645 must complete a timing cycle before the GATE pin voltages are allowed to rise. This allows the connector pins to finish bouncing and make a solid connection. C_{TIMER} charges to 1.23V with a 2µA current source, setting the delay timing cycle equal to t = (1.23V • C_{TIMER})/2µA. In this example, the undervoltage lock-

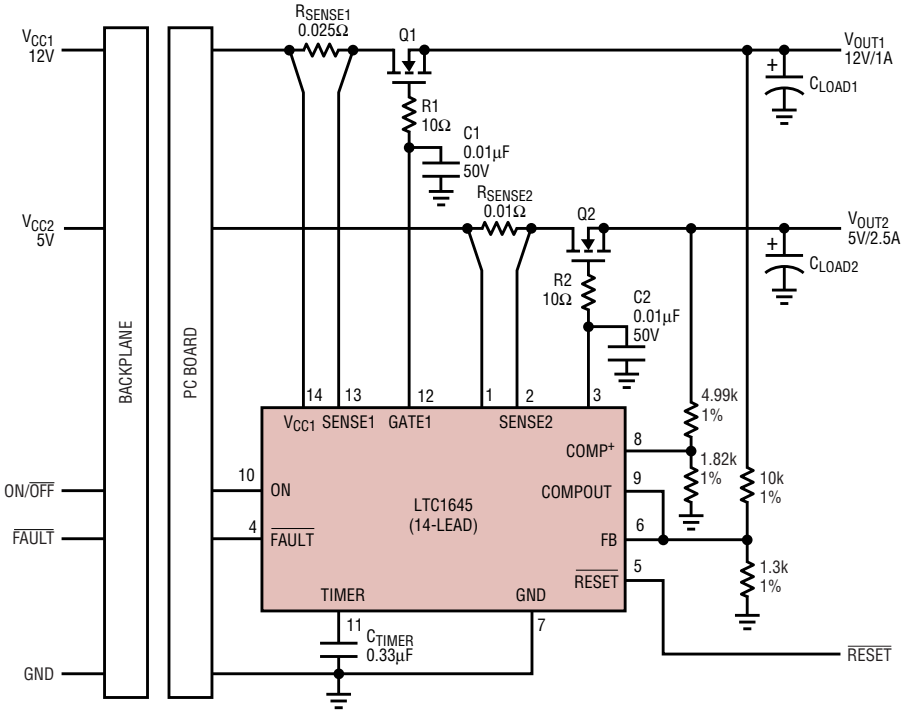

Figure 1. LTC1645 typical application

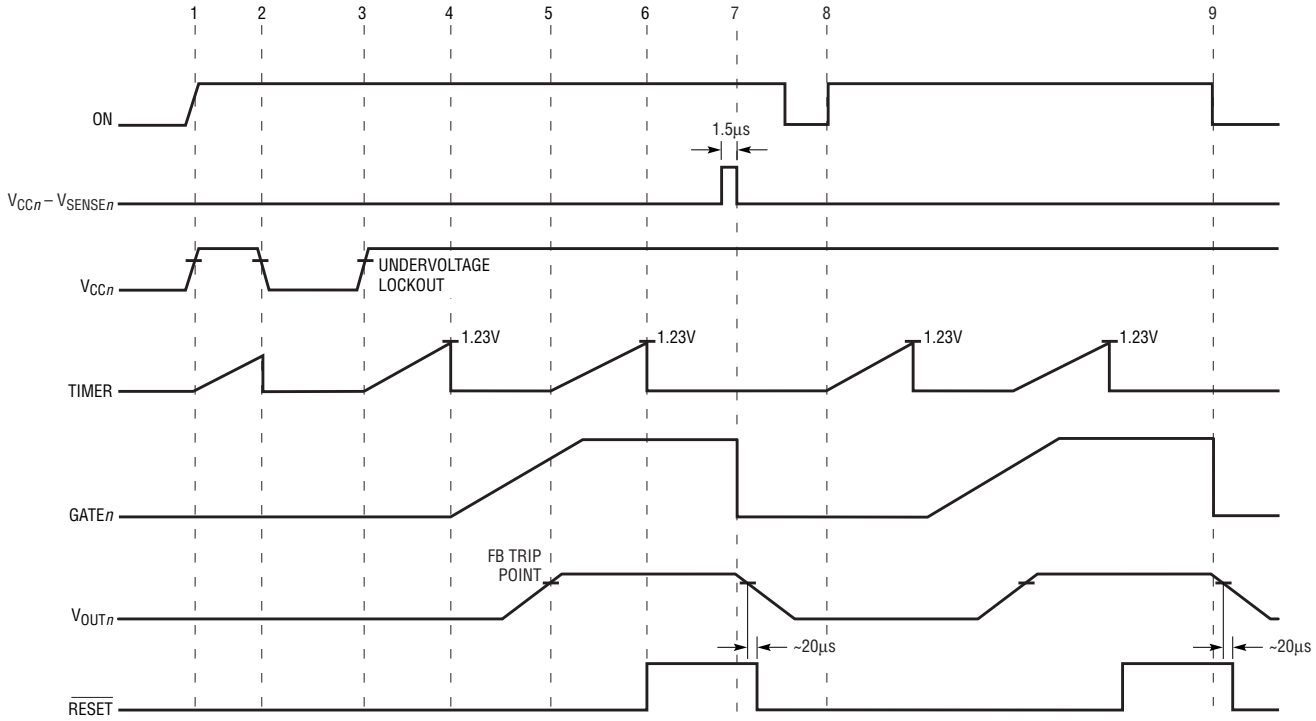

Figure 2. Typical insertion and electronic-circuit-breaker timing

out circuit discharges the TIMER pin and prevents both channels from turning on when $V_{CC1} < 2.23V$ or $V_{CC2} < 1.12V$ (time point 2). At time point 4, the timing cycle is completed and the GATE pins are pulled up by an internal 10µA current source; the voltage at GATE1 begins to rise with a slope of 10µA/C1 and the voltage at GATE2 begins to rise with a slope of 10µA/C2. The supply voltages follow their respective gate voltages minus the external FET threshold voltage; the ramp time for each supply is $(V_{CCn} \bullet Cn)/10\mu A$.

Voltage Monitor and Spare Comparator

The 14-pin version of the LTC1645 provides two precision comparators for monitoring input or output voltage levels. Both comparators have a 1.238V reference as the negative input and have open-drain outputs that require an external pull-up to generate a logic high. The spare comparator monitors COMP+ and releases COMPOUT immediately whenever COMP+ is above 1.238V. The FB comparator releases RESET one timing cycle after the FB pin rises above 1.238V (Figure 2, time points 5 and 6) and includes a glitch filter to prevent system resets during short negative transients on the FB pin. The filter time is 20µs for large transients (greater than 150mV) and up to 100µs for smaller 10µA transients.

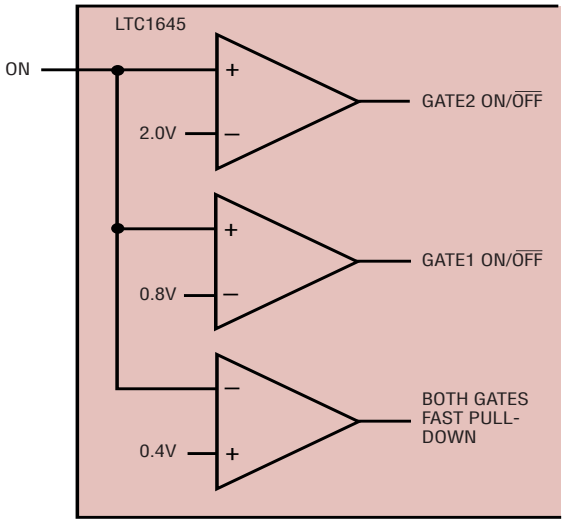

Figure 3. On-pin operation

In Figure 1, the COMPOUT pin has been tied to the FB pin so that RESET will not release until both output supplies remain above their programmable voltages for one timing cycle.

Electronic Circuit Breaker

The LTC1645 features an electronic circuit breaker function that protects against short circuits or excessive output current. Load current for each supply is monitored by a sense resistor between the supply input and sense pin of the chip. The circuit breaker trips whenever the voltage across the sense resistor exceeds 50mV for more than 1.5µs. When the circuit breaker of either channel trips, both GATE pins are immediately pulled to ground and the external FETs are quickly turned off (Figure 2, time point 7). When the ON pin is cycled off and on (time point 8), the circuit breaker resets and another timing cycle starts. If the circuit breaker feature is not required, short the SENSE pins to their respective V_{CC} pins.

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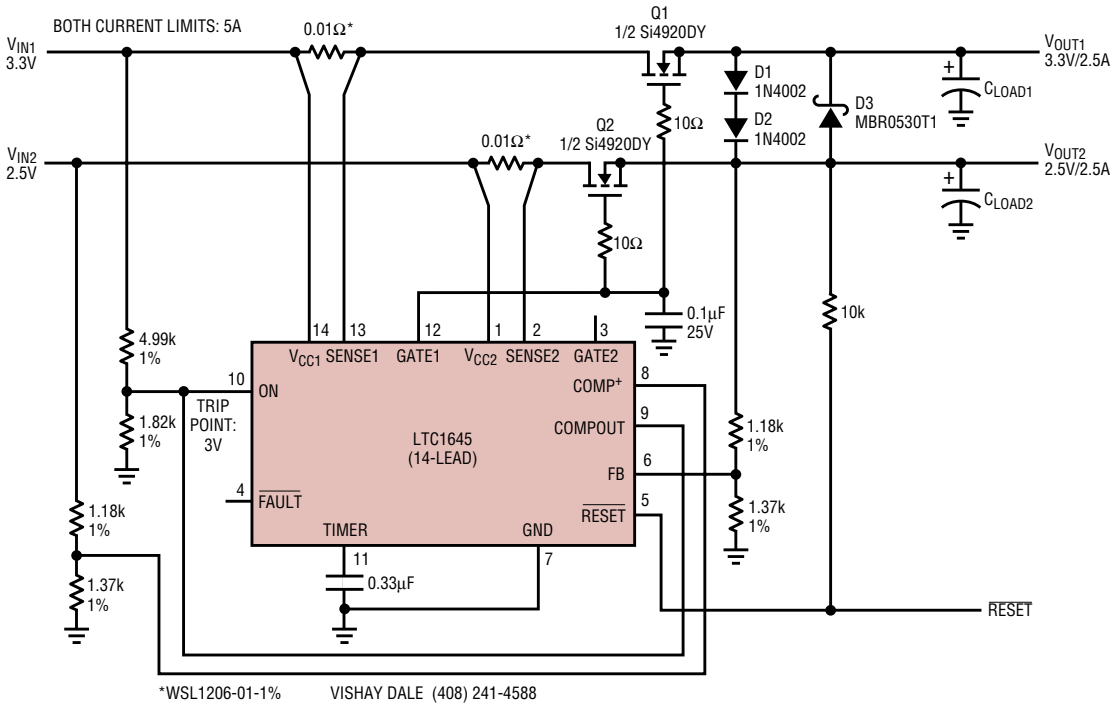

Figure 4. Ramping 3.3V and 2.5V up and down together

The ON Pin

The ON pin has multiple thresholds to control the ramping up and down of the GATE*n* pins. Figure 3 is a block diagram showing operation of the ON pin. If the ON pin voltage is below 0.4V, GATE1 and GATE2 are immediately pulled to ground. While the voltage is between 0.4V and 0.8V, GATE1 and GATE2 are each pulled to ground with a 40µA current. Between 0.8V and 2V, the GATE1 10µA pull-up is turned on after one timing cycle, but GATE2 continues to be pulled to ground with a 40µA current. When the voltage exceeds 2V, both the GATE1 and GATE2 10µA pull-ups are turned on one timing cycle after the voltage exceeds 0.8V.

Power Supply Tracking and Sequencing

Some applications require that the difference between two power supply voltages not exceed a certain value. This requirement applies during power-up and power-down, as well as during steady state operation; often this is done to prevent latch-up in a dual-supply ASIC. Other systems require one supply to come up after another, for example, when a system clock needs to start before a block of logic. Typical dual supplies or backplane connections may come up at arbitrary rates depending on load current, capacitor size, soft-start rates and so on. Traditional solutions can be cumbersome or require complex circuitry to meet the necessary requirements.

The LTC1645 provides simple solutions to power supply tracking and sequencing needs. The LTC1645 can guarantee supply tracking by ramping the supplies up and down together and allows nearly any combination of supply ramping to satisfy various sequencing specifications. Figure 4 shows an application ramping V_{OUT1} and V_{OUT2} up and down together. The ON pin must reach 0.8V to turn on GATE1, which ramps up V_{OUT1} and V_{OUT2}. The spare comparator pulls the ON pin low until V_{CC2} is above 2.3V, and the ON pin cannot reach 0.8V before V_{CC1} is above 3V.

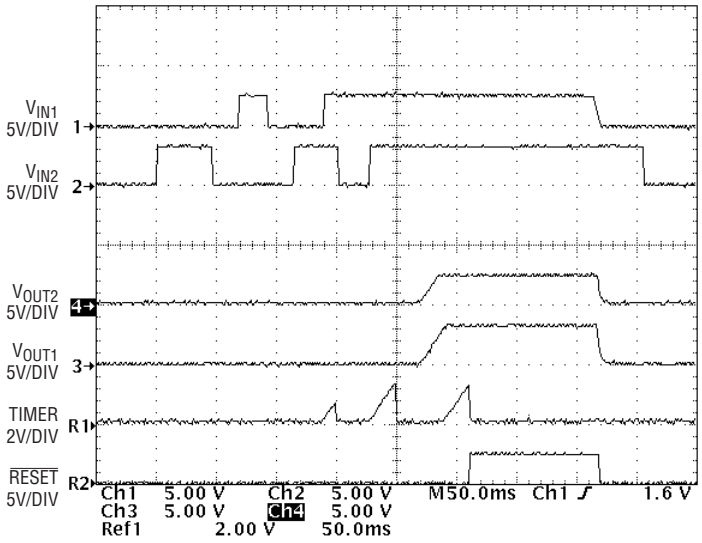

Figure 5. Input, output and control signals of Figure 4's circuit

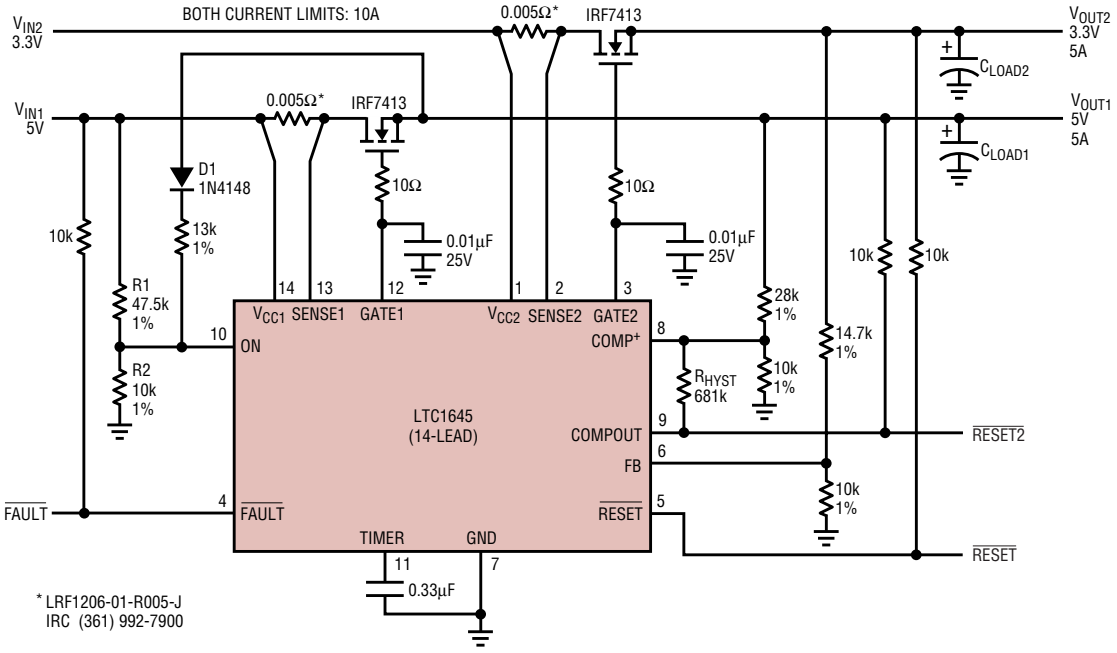

Figure 6. Ramping up 5V followed by 3.3V

Thus, both input supplies must be within regulation before a timing cycle can start. At the end of the timing cycle, the output voltages ramp up together. If either input supply falls out of regulation or if an overcurrent condition is detected, the gates of Q1 and Q2 are pulled low together.

Figure 5 shows an oscilloscope photo of of Figure 4's circuit in action. On power-up, V_{OUT1} and V_{OUT2} ramp up together. On power-down, the LTC1645 turns off Q1 and Q2 simultaneously. Charge remains stored on C_{LOAD1} and C_{LOAD2} and the output voltages will vary depending on the loads. D1 and D2 turn on at ≈1V (≈0.5V each), ensuring that V_{OUT1} never exceeds V_{OUT2} by more than 1.2V, while D3 guarantees that V_{OUT2} is never greater than V_{OUT1} by more than 0.4V. Barring an overvoltage condition at the input(s), the only time these diodes can conduct current is during a power-down event, and then only to discharge C_{LOAD1} or C_{LOAD2}. In the case of an input overvoltage condition that causes excess current to flow, the circuit breaker will trip if the current limit level is set appropriately.

Figure 6 shows the LTC1645 configured to ramp up V_{OUT1} before V_{OUT2}. C_{LOAD1} is initially discharged and D1 is reverse-biased, thus the voltage at the ON pin is determined only by V_{CC1} through the resistor divider R1 and R2. If V_{CC1} is above 4.6V, the voltage at the ON pin exceeds 0.8V and V_{OUT1} ramps up one timing cycle later. As V_{OUT1} ramps up, D1 forward-biases and pulls the ON pin above 2V when V_{OUT1} ≈ 4.5V. This turns on GATE2 and V_{OUT2} ramps up. The FB comparator monitors V_{OUT2}, and the spare comparator monitors V_{OUT1} with R_{HYST} creating ~50mV of hysteresis. To ensure that V_{OUT1} does not fall much below V_{OUT2} as the load capacitors discharge during power down, a Schottky diode can be connected from V_{OUT2} to V_{OUT1}.

Conclusion

Designing a traditional hot-insertion system requires a significant effort by an experienced analog designer. An easy way to reduce the design effort is to use the LTC1645, which offers charge-pump gate drivers, a user programmable delay, voltage level monitors and other specialized features. With the LTC1645, it is easy to create reliable Hot Swap systems.

For more information on parts featured in this issue, see http://www.linear-tech.com/go/ltmag

LTC1642: a Hot Swap Controller with Foldback Current Limiting and Overvoltage Protection

by Pat Madden

Hot Circuit Insertion

When a circuit board is inserted into a "hot" (powered) backplane, its supply bypass capacitors can draw large currents from the backplane power bus as they charge. These currents can cause glitches on the backplane supply voltage, resetting other boards in the system, and can even destroy edge connectors. Like other members of Linear Technology's Hot Swap family, the LTC1642 limits the charging current drawn by a board's capacitors, allowing safe circuit board insertion into a hot backplane. It also offers additional capabilities, some new to the Hot Swap family: a maximum recommended operating voltage of 16.5V, a programmable electronic circuit breaker with foldback current limiting, overvoltage protection to 33V, and a voltage reference and uncommitted comparator.

In the circuit shown in Figure 1, the LTC1642 and the external NMOS pass transistor Q1 work together to limit the charging current when a board is plugged into a hot backplane. In this application, the backplane voltage is 12V, but the chip will operate with any supply voltage between 3.0V and 16.5V. When power is first applied to V_{CC}, the chip holds Q1's gate at ground. After a programmable debounce delay, an internal 25µA current source begins to charge the external capacitor C2, generating a voltage ramp of 25µA/C2 V/s at the GATE pin. Because Q1 acts as a source follower while its gate ramps, the current charging the board's bypass capacitance, C_{LOAD}, is limited to 25µA • C_{LOAD}/C2. An internal charge pump supplies the 25µA gate current, ensuring sufficient gate drive to Q1. Resistor R3 protects against high frequency FET oscillations; capacitor C1 sets the debounce delay, ΔT_D, before the GATE pin voltage begins ramping: ΔT_D(ms) = 615 • C1(µF). The ON pin is the chip's control input; when it is below 1.22V, the GATE pin is held at ground. If ON/OFF control of the LTC1642 is not required, ON should be tied to V_{CC} through a 50k current limiting resistor. Typical waveforms at card insertion are shown in Figure 2.

Short-Circuit Protection

A short circuit from Q1's source to ground can destroy the FET; it can also reset every other card in the system if the backplane supply voltage droops due to the excessive current. The LTC1642 can protect against both threats by limiting the current drawn from the backplane supply during a short circuit and by opening an electronic circuit breaker before Q1 overheats. The addition of analog current limiting to the standard electronic circuit breaker function can improve system performance. For example, consider a system of plug-in cards powered by a backplane supply. The sudden removal of one card causes the backplane voltage to ring at a fairly high frequency, due to the step change in supply current. This ringing signal appears differentially across the sense

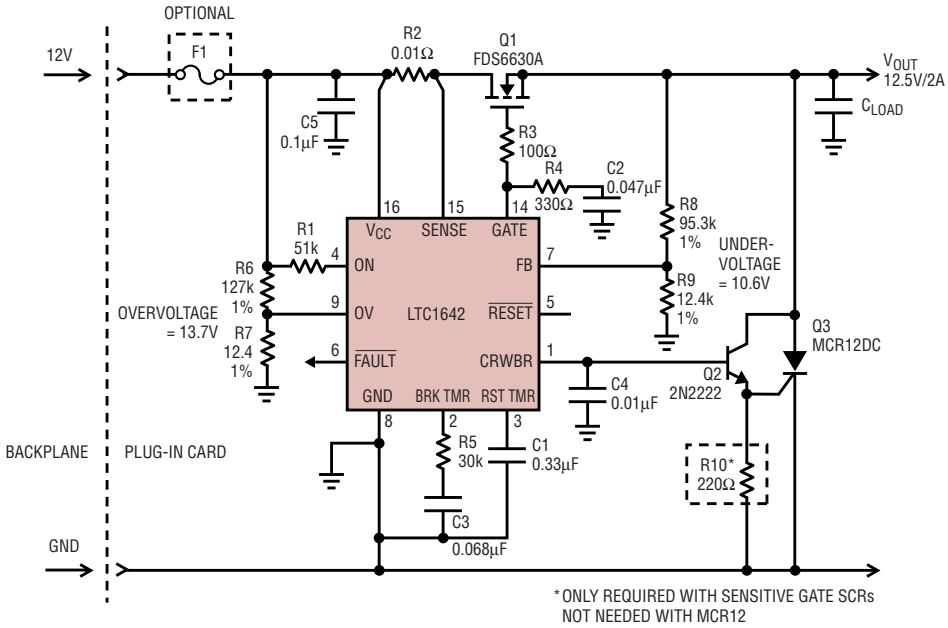

Figure 1. Typical LTC1624 Hot Swap application

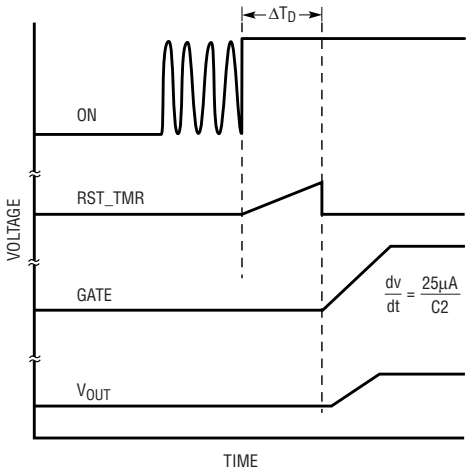

Figure 2. Typical waveforms at card insertion

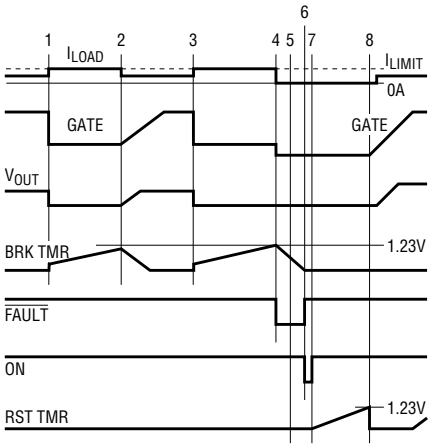

Figure 3. Current-limit and circuit-breaker timing

resistor on each remaining card. It can trip the circuit breaker, even though there is no fault on the card. To prevent this, the designer may attempt to slow the circuit breaker by connecting a lowpass RC network across the sense resistor, only to find that one problem has been exchanged for another: if there is a short circuit on the card, the backplane voltage droops too much before the circuit breaker opens. The LTC1642 shines in this application. It regulates the load current within a few microseconds after a short circuit, before the backplane can droop, but can delay opening the circuit breaker for milliseconds or more, which allows the ringing to decay, resulting in almost complete immunity from backplane noise.

The external components that provide short-circuit protection are included in Figure 1. R2 senses the load current, and, if its voltage drop reaches the internal threshold, the current-limit servo loop adjusts the GATE pin voltage such that Q1 acts as a constant current source. R2's voltage limit decreases as the output voltage decreases; this "foldback" tends to keep Q1's power dissipation constant in current limit. The output voltage is sensed at the FB pin. When FB is grounded, the internal threshold voltage is 20mV, but this increases gradually to 50mV with increasing voltage at FB. To compensate this servo loop R4 is added in series with C2; to ensure stability, the product $1/(2 \bullet \pi \bullet R4 \bullet C2)$ should be kept below the loop's unity-gain frequency of 125kHz and C2 should be larger than Q1's input capacitance, C_{ISS}. The values shown in Figure 1, C2 = 0.047µF and R4 = 330Ω, work well with the Fairchild FDS6630A and similar MOSFETs. The $\overline{\text{FAULT}}$ output, when asserted, signals that the circuit breaker has opened. Capacitor C3 and resistor R5 set the delay, ΔT_{BRK}, between the onset of current limiting and the circuit breaker opening: $\Delta T_{BRK}(ms) = [62 - R5(k\Omega)] \bullet C3(\mu F)$. R5 slows C3's discharge, ensuring that the circuit breaker eventually opens in the event of repetitive, but short, current faults. These are dangerous because the slow voltage ramp at Q1's gate means that it continues to dissipate substantial power for some time after the current limit clears. Larger values of R5 protect against lower duty cycle shorts, at the cost of greater uncertainty in the circuit breaker delay time. A prudent upper limit on R5 is 30k, which will open the circuit breaker if the duty cycle of a repetitive short exceeds 50%.

Typical waveforms during a short circuit are shown in Figure 3. The load is shorted to ground at time 1. The GATE voltage drops until Q1 comes into regulation and the circuit breaker timer (BRK TMR) starts. The short is cleared at time 2, before the breaker opens, and the GATE voltage ramps back up. At time 3, the load is shorted again and at time 4 the breaker opens, pulling the GATE to ground and asserting $\overline{\text{FAULT}}$. Although the short is cleared at time 5, $\overline{\text{FAULT}}$ doesn't go high until time 6 (it has an internal 10µA pull-up), after the ON pin has been low for two microseconds. At time 7, ON goes high and the debounce timer (RST TMR) starts; at time 8 the GATE voltage begins ramping.

Powering Up in Current Limit

Ramping the GATE pin voltage *indirectly* limits the charging current to $I = 25\mu A \bullet C_{LOAD}/C2$, where C2 is the external capacitor connected to the GATE and C_{LOAD} is the load capacitance. If the value of C_{LOAD} is uncertain, a worst-case design can result in needlessly long ramp times and it may be better to limit the charging current *directly* by allowing the LTC1642 to power up in current limit. This is perfectly acceptable as long as the circuit breaker delay is long enough to power up under worst-case conditions.

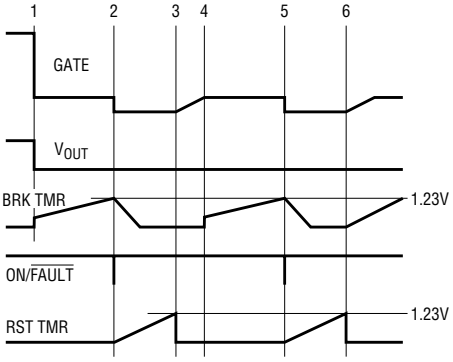

Figure 4. Automatic restart following a short circuit

Automatically Restarting after the Circuit Breaker Opens

The LTC1642 will automatically attempt to restart itself after the circuit breaker opens if the $\overline{\text{FAULT}}$ output is tied to the ON pin input. The resulting waveforms during a short circuit are shown in Figure 4. As the figure shows, pass transistor Q1's duty cycle is equal to the circuit breaker delay, ΔT_{BRK}, divided by the sum of the circuit breaker and debounce delays, $\Delta T_{BRK} + \Delta T_D$. Q1 dissipates substantial power while acting as a constant current source, so be sure its maximum junction temperature is not exceeded in worst-case conditions. For example, the FDS6630A in Figure 1 dissipates 24W(= 2A • 12V) DC when the load is shorted to ground. Its absolute maximum junction temperature, T_J, is 150°C, so an ambient temperature, T_A, of 85°C requires an effective junction-to-ambient thermal resistance of 2.7°C/W $(= (T_J - T_A)/(I \bullet V))$ or less. The effective junction-to-ambient thermal resistance is the product of two factors: θ_{JA}, the DC junction-to-ambient thermal resistance, which depends on the package and board layout; and *r(t)*, a

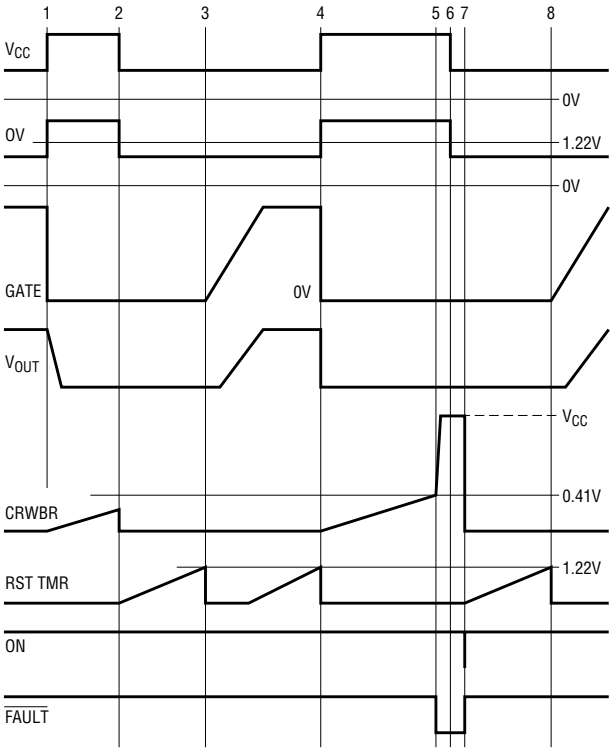

Figure 5. Overvoltage timing

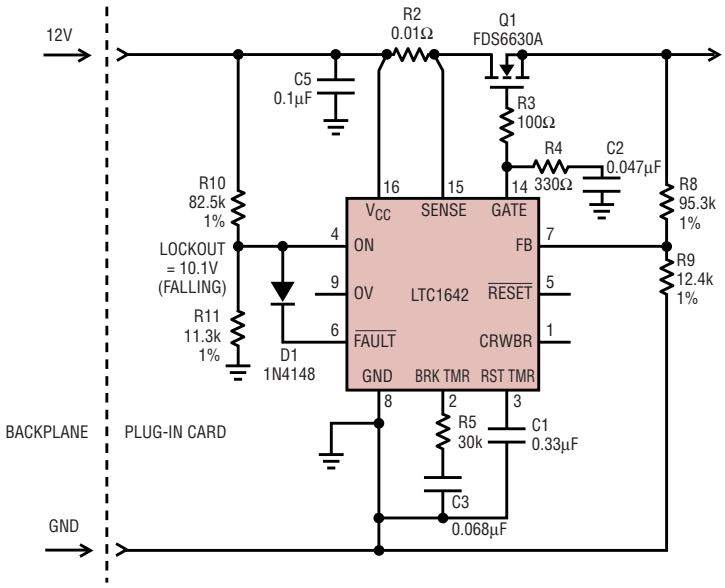

Figure 6. Increasing the undervoltage lockout threshold

derating factor that depends on the transistor's duty cycle and "on" time. Referring to the FDS6630A's data sheet, a 0.2in^2 mounting pad of 2oz. copper on an FR-4 board produces a DC thermal resistance, θ_{JA}, of 105°C/W; referring to Figure A (Transient Thermal Response Curve—reproduced from the FDS6630A data sheet), a 2ms circuit breaker delay and a 200ms debounce delay produce an *r(t)* derating of 0.02; the overall effective thermal resistance is 2.1°C/W (= *r(t)* • θ_{JA}).

If $\overline{\text{FAULT}}$ is tied to ON, open-drain logic should be used to drive the node, and the external pull up resistor at the ON pin may be omitted, because $\overline{\text{FAULT}}$ provides a weak internal pull-up.

Overvoltage Protection

The LTC1642 can protect a card from excessive voltage by quickly turning off the pass transistor if the supply voltage exceeds a programmable limit and by triggering a crowbar SCR after a programmable delay. The LTC1642 includes an internal regulator that protects against supply voltages up to 33V. It can also be configured to automatically restart when an overvoltage condition clears.

The external components that provide overvoltage protection are included in Figure 1. Resistors R6 and R7 set the overvoltage limit, timing capacitor C4 sets the delay before the crowbar SCR Q3 fires and NPN follower Q2 boosts the trigger current into Q3. When V_{CC} exceeds (1 + R6/R7) • 1.22V, an internal comparator trips and the chip cuts off Q1 by pulling its gate to ground. For better noise rejection, the propagation delay through the comparator (on a low-to-high transition at OV) increases from 20µs to 80µs as the differential input voltage decreases from 175mV to 3mV. Once the comparator trips, an internal 45µA current starts charging C4; when it reaches 0.41V the current increases to 1.5mA and Q2 quickly triggers the SCR. The delay, ΔT_{SCR}, before the SCR triggers is ΔT_{SCR}(ms) =

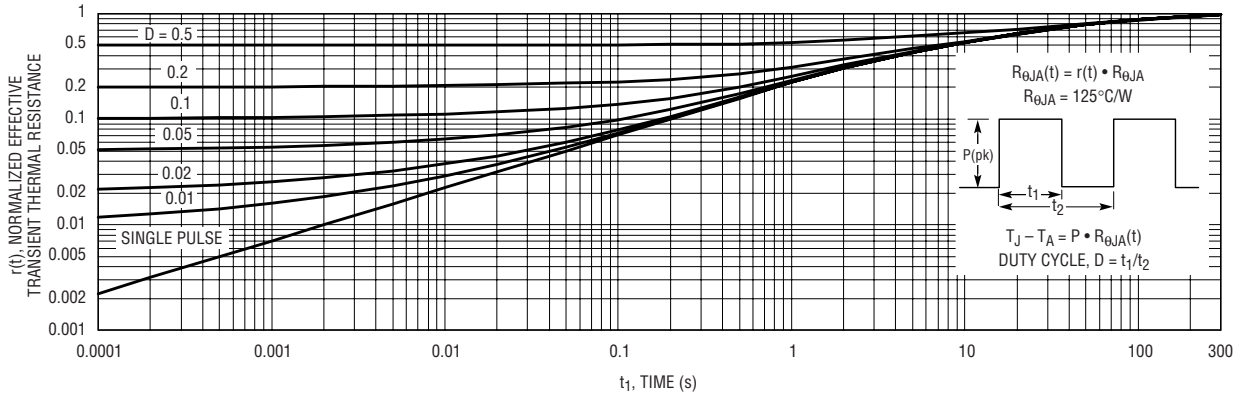

Figure A. Fairchild FDS6630A transient thermal response curve (reproduced by permission, from the FDS6630A data sheet)

9 • C4(µF). Once C4 reaches 0.41V, the LTC1642 latches off. After the overvoltage clears, GATE and FAULT remain at ground and the 1.5mA charging current persists. To restart after the overvoltage clears, hold the ON pin low for at least 2µs and then bring it high. The GATE voltage will begin ramping up after a debounce delay. The chip will restart if FAULT and ON are connected together: the GATE voltage begins ramping up one debounce delay after the overvoltage clears.

Figure 5 shows typical waveforms. The OV comparator goes high at time 1, causing the chip to pull the GATE pin to ground and start charging C4. At time 2, before the capacitor reaches 0.41V, OV falls below 1.22V; C4 discharges and the GATE voltage begins ramping after the debounce delay ends at time 3. Another overvoltage begins at time 4, and at time 5 C4 reaches 0.41V; FAULT goes low and the charging current increases to 1.5mA. Even after OV falls below 1.22V at time 6, GATE and FAULT stay low and CRWBR continues to source 1.5mA. FAULT goes high when ON goes low momentarily at time 7; after a debounce delay ending at time 8, the GATE voltage begins ramping.

The LTC1642's internal regulator turns on when V_{CC} exceeds 17.5V and turns off when it drops below 17.0V. While on, it limits the internal supply voltage to most of the chip's circuits to 15V. They will function normally except that the GATE pin charge pump is disabled. Set the resistor divider at the OV pin to ensure that GATE is grounded with V_{CC} levels above 16.5V.

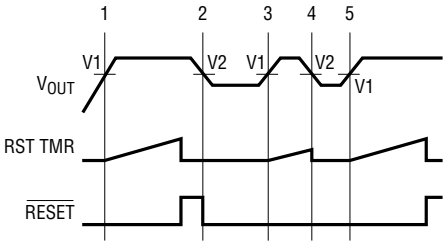

Figure 7. Undervoltage monitor waveforms

Undervoltage Lockout

An internal undervoltage lockout circuit keeps the GATE pin at ground until V_{CC} exceeds 2.73V. If it falls below 2.5V, the lockout circuit pulls GATE to ground and resets the circuit breaker and SCR trigger. To set a higher lockout voltage, tie the ON pin to a resistor divider driven from V_{CC}, as shown in Figure 6. The chip remains locked out until V_{CC} exceeds (1 + R10/R11) • 1.33V and will also lock out if V_{CC} falls below (1 + R10/R11) • 1.22V. If the resistive divider is used in conjunction with automatic restart, connect FAULT to ON through a diode, as shown. Otherwise FAULT's internal pull-up current, which varies with operating voltage and temperature, will skew the lockout threshold.

Undervoltage Monitor

In Figure 1, the LTC1642's FB pin monitors the output voltage; the chip asserts RESET if the output falls below 1.22V • (1 + R8/R9) (10.6V for the R8 and R9 values in the figure). RESET goes high (it has a 10µA internal pull-up) when the output has continuously exceeded this voltage for one debounce delay. Typical waveforms are shown in Figure 7. On power-up, RESET is asserted; it remains low until one debounce delay (ΔT_D(ms) = 615 • C1(µF)) after FB crosses 1.22V at time 1. At time 2, FB falls below 1.22V and RESET is asserted immediately. When FB exceeds its threshold at time 3, the debounce timer starts, but FB falls below 1.22V (time 4) before the debounce delay ends and RESET remains low. FB crosses 1.22V once more at time 5 and RESET goes high one debounce delay later. To improve noise rejection, the FB comparator's propagation delay (on a falling edge at FB) increases from 20µs to 80µs as the differential input voltage decreases from 175mV to 3mV.

Reference and Uncommitted Comparator

The LTC1642's internal voltage reference is buffered and brought out to the REF pin. The buffer amplifier should be compensated with a capacitor connected between REF and ground. If no DC current is drawn from REF, 0.1µF ensures an adequate phase margin, but larger capacitors can be used for better suppression of high frequency noise on REF.

The LTC1642 also includes an uncommitted comparator with an open drain output and a common mode input range includes ground.

Conclusion

The LTC1642 is a rugged Hot Swap controller that can handle positive supplies up to 15V. It also provides fast, effective current limiting even in the presence of a noisy backplane supply and can protect plug-in cards against overvoltages up to 33V.

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Cost and Space Efficient Backlighting for Small LCD Panels

by Jim Williams

A generation of small, portable, "palmtop" computing devices has recently appeared. These products have small LCD displays that use cold cathode fluorescent lamps (CCFLs) for backlighting. These lamps require high voltage AC current drive. Circuitry for this purpose should be physically small, cost effective and electrically efficient.

Figure 1 shows a design that meets the above criteria. The configuration is a current-fed resonant Royer converter driven by an LT1317B micropower switching regulator. The LT1317B effects a switch-mode current sink, supplying the required Royer drive to close a loop at the FB pin. This path includes the lamp and a filter network that rectifies T1's high voltage AC output into DC. In this case, the circuit's operating point, and hence, the lamp current, is set by a potentiometer. Operating-point variation can also be achieved by voltage controlling the optional input, indicated on the schematic.[1] With the components shown, size is about 10mm (W) by 5mm (H) by 40mm (L). The Shutdown pin facilitates circuit turnoff, although removing power from the V_{IN} pin has similar results.

The closed loop operation yields excellent line regulation while ensuring that lamp currents never violate minimum or maximum values. These characteristics allow operation directly from the battery without intensity variation, flicker or shortening of lamp life. Simplicity, low component count, small size and cost effectiveness make this circuit an excellent choice for "palmtop" LCD illumination.

[1] Those finding this description intolerably brief are directed to LTC Application Note 65, where this circuit receives more scholarly attention.

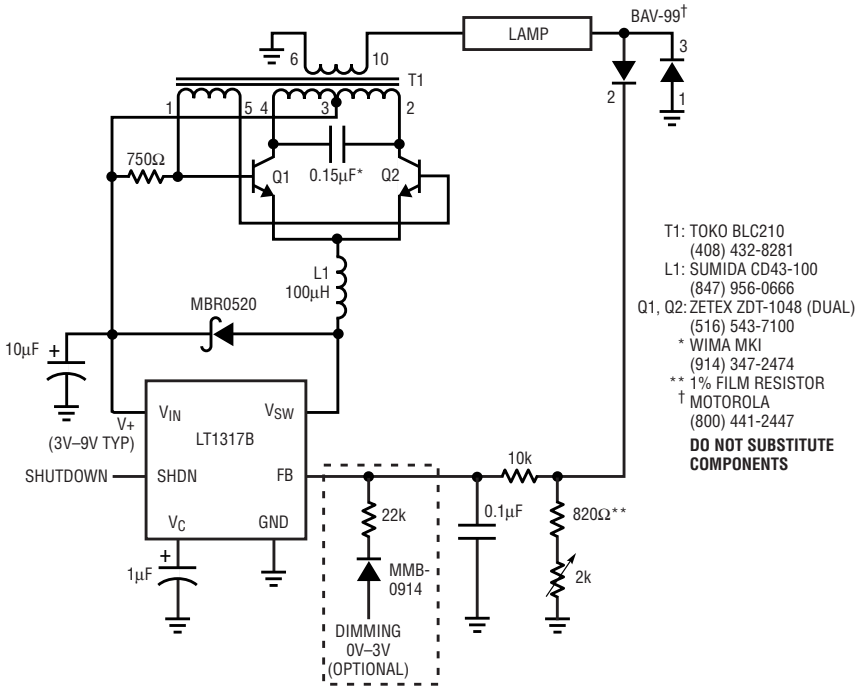

Figure 1. Palmtop computer LCD backlight supply

For more information on parts featured in this issue, see http://www.linear-tech.com/go/ltmag

High Efficiency PolyPhase Converter Combines Power from Multiple Inputs

by Wei Chen and Craig Varga

Introduction

As more functions are integrated into one IC, the power drawn by a single IC can easily exceed the capability of a single input power source. One solution is to use several available power sources to obtain the required output power, drawing some percentage of the total power from each source. The LTC1929 PolyPhase™ controller provides a simple solution to this problem.

Design Details

The LTC1929 is a PolyPhase dual, current mode controller. It is capable of driving two synchronous buck channels 180 degrees out of phase to reduce output switching ripple current and voltage. One buck stage receives its input power from the 12V input and the other receives its power from the 5V input. In a 2-phase design, as the inductor current in the 5V circuit increases, the inductor current in the 12V circuit decreases. This results in a smaller net ripple current flowing into the output capacitor. Since there are two intervals in one switching period where ripple cancellation takes place, the output ripple voltage of the 2-phase design is much smaller than that of a single-phase design and fewer output capacitors can be used.

A Typical Application

The currents available from a PCI connector are limited to 2A for the 5V supply and 1A for the 12V supply. In the example shown here, the load can be as high as 6A or 16.8W at 2.8V. Neither the 5V nor the 12V source is capable of providing this power. Hence, it is desirable to design a power supply that can draw currents from two power sources and whose maximum input currents from each source will not exceed the corresponding limit. With only one IC, two SO-8 MOSFETs and two small inductors, a high efficiency, low noise power supply can be built.

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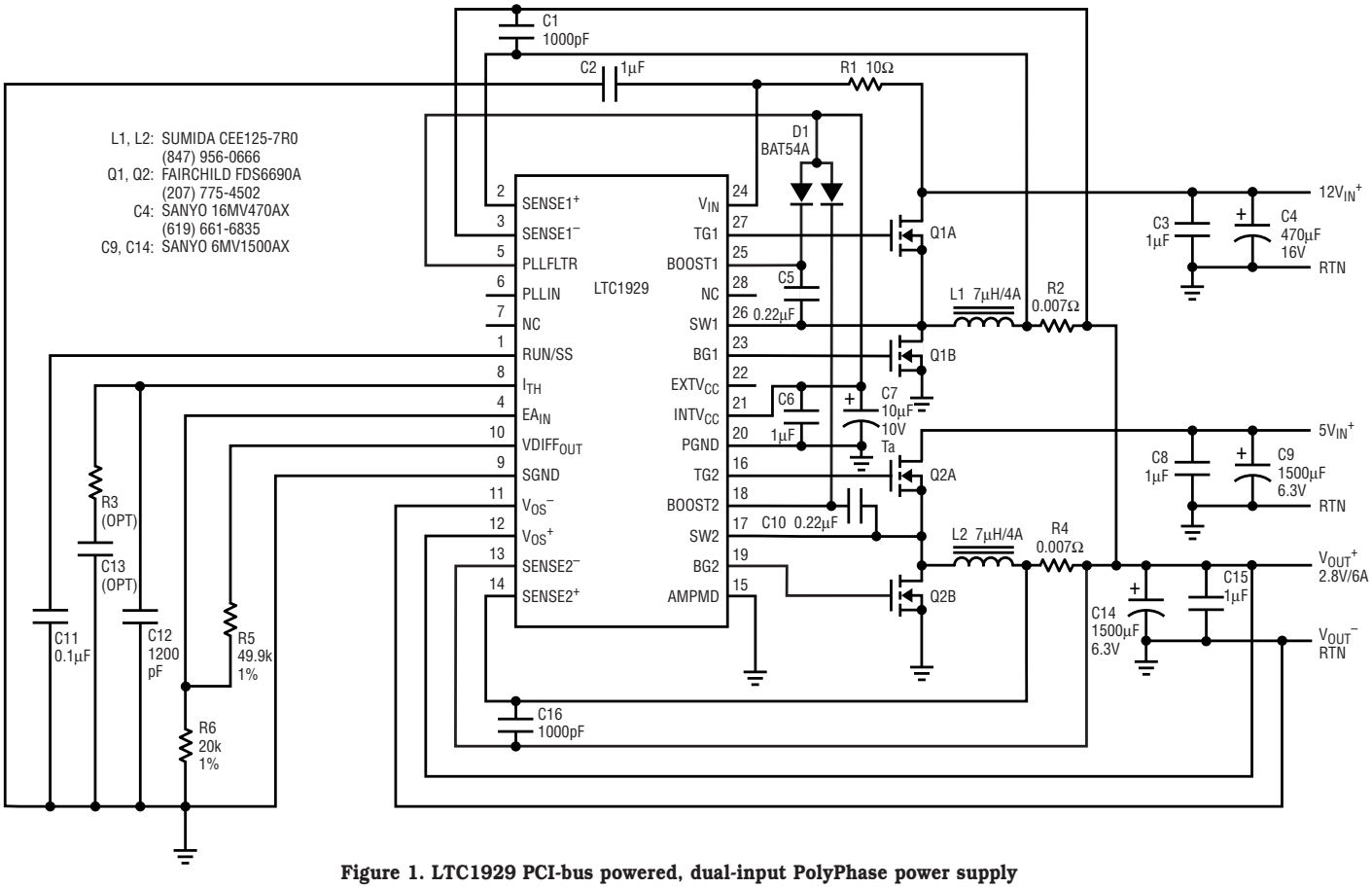

Figure 1. LTC1929 PCI-bus powered, dual-input PolyPhase power supply

Isolated RS485 Transceiver Breaks Ground Loops

by Mitchell Lee

The RS485 interface is designed to handle a –7V to 12V input signal range; however, in practical systems, ground potentials vary widely from node to node, often exceeding the specified range. This can result in an interruption of communications, or worse, destruction of a transceiver. Guarding against large ground-to-ground differentials calls for an isolated interface. A new surface mount device, the LTC1535 isolated RS485 transceivers, provides a one-chip solution for breaking ground loops.

Previously, isolation was achieved using at least three optoisolators and a separate isolated power supply. The LTC1535 replaces not only the optoisolators, but also the power supply, as it includes an on-chip DC/DC converter. Other features include selectable driver slew rate to reduce EMI and susceptibility to reflections, full-duplex pinout and fail-safe detection of open and shorted lines.

The LTC1535 consists of two separate dice assembled on a proprietary, isolated lead frame. The lead frame includes integral coupling capacitors that bridge the isolation barrier and exhibit 2,500V_{RMS} guaranteed standoff. Data communication takes place via the coupling capacitors, while an on-chip, 400kHz push-pull switching regulator sends power to the isolated side through a small transformer. Total common-mode capacitance across the barrier amounts to less than 20pF, with the transformer accounting for about 16pF of the total. Figure 1 shows the complete circuit for a fully isolated RS485 port.

The two halves of the LTC1535 communicate in a ping-pong fashion, first sending transmit data to the isolated side and then sending receive data back to the nonisolated side. The sampling nature of the internal communications link means that some jitter is introduced into the data; this limits the useful baud rate to approximately 500kBd. At 350kBd, the jitter is guaranteed to be less than 10%. Figure 2 shows a double pulse propagating through the LTC1535. Waveform (A) is the transmitter data input and waveform (B) is the output of the receiver. The transmitter and receiver are looped back on the isolated side of the chip. The typical jitter is hardly visible. A negative-going double pulse is shown in Figure 3. The LTC1535 transceiver is unaffected by the DC average of the data waveform. Total round-trip propagation delay through the LTC1535 is approximately 1µs or roughly equivalent to 328 feet of cable.

Figure 4 shows the driver output waveform when loaded by 5000' of terminated cable, operating in the fast slew mode (SLEW pin pulled high). The effect of the SLEW pin on the driver output waveform is noticeable in Figure 5, where rise and fall times of approximately 1µs result.

Isolation can bring potentially dangerous voltages onto a circuit board and within easy reach of the end user. For example, if the twisted pair is accidentally miswired or faults to 117V at some remote location, the floating section of each LTC1535 and its associated circuitry will also carry 117V. An unwary user or installer could then come in contact with what is assumed to be a safe, low voltage circuit. Figure 6 shows how to detect and warn the user that a fault condition exists on the twisted pair or its shield. A small (3.2mm) glow lamp is connected between GND2 (the LTC1535's floating ground) and the equipment's safety "earth" ground. If a potential of more than 75VAC is present on the twisted pair or shield, B1 will light, indicating a wiring fault. Resistors R3 and R4 are used to ballast the current in B1. Two resistors are necessary because each resistor can only stand off 200V, as well as for reasons of power dissipation. As shown, the circuit can withstand a direct fault to a 440V, 3-phase system.

Other problems introduced by floating the twisted pair include the collection of static charge on the twisted pair, its shield and the

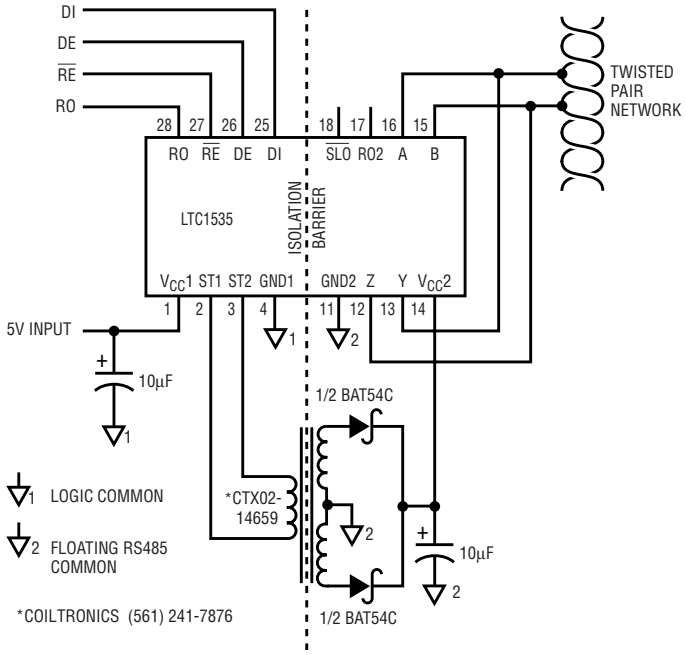

Figure 1. Fully isolated RS485 port

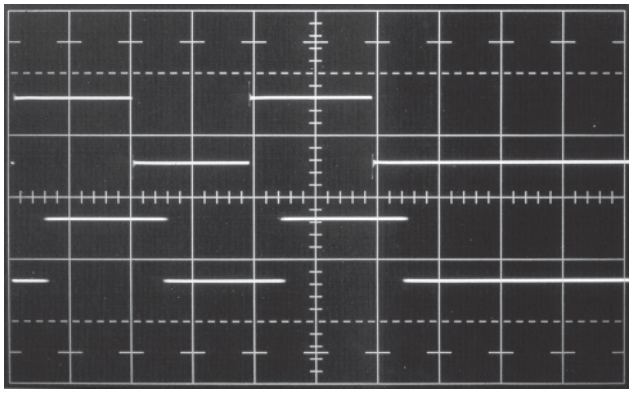

Figure 2. Positive-going double-pulse behavior: A = driver input, B = receiver output

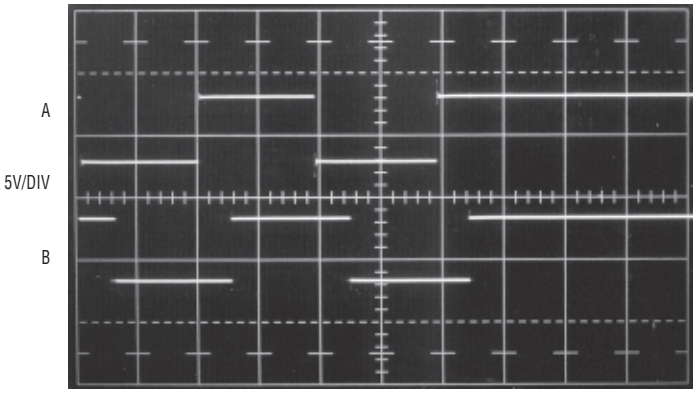

Figure 3. Negative-going double-pulse behavior: A = driver input, B = receiver output

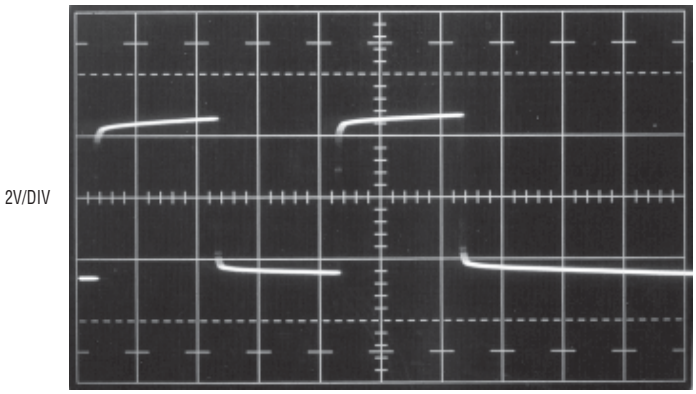

Figure 4. Driver in fast slew mode, loaded with 5000' of twice-terminated twisted pair

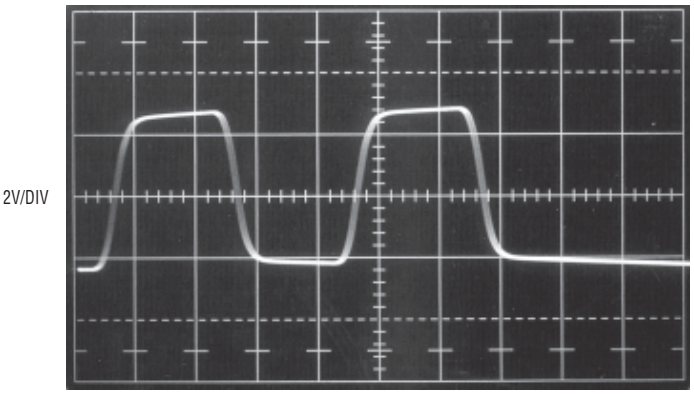

Figure 5. Driver in slow slew mode, loaded with 5000' of twice-terminated twisted pair

attached circuitry. R1 and R2 provide a path to shunt static charge safely to ground. Again, two resistors are necessary to withstand high voltage faults. Electrostatic spikes and transients can temporarily elevate the twisted pair to 10kV or more. C1 in Figure 6 absorbs this charge and limits the peak voltage that reaches the LTC1535 to a safe value. As an example, if a 1000pF source charged to 10kV comes in contact with the cable, a single 10nF capacitor at C1 will reduce the peak voltage to just 1kV, decaying in less than 10ms through R1–R4 and B1. 1kV is well within the capabilities of the LTC1535.

Combining isolation, power and a fully-compliant RS485 transmitter and receiver, the LTC1535 provides a compact, cost-effective solution for isolated serial data communications.

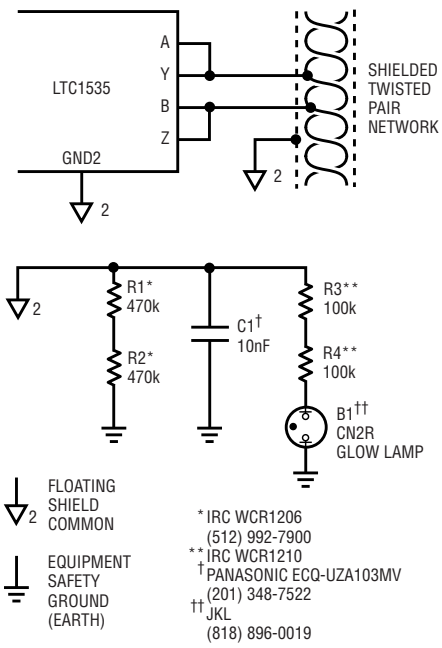

Figure 6. Detecting wiring faults

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Sharp Gain Roll-Offs Using the LTC1562 Quad Operational Filter IC (Part 3)

by Nello Sevastopoulos

This is the third in series of articles describing applications of the LTC1562 quad Operational Filter™ IC connected as a lowpass, highpass, notch or bandpass filter with added stopband notches to increase selectivity.

Parts 1 and 2 of the series (*Linear Technology* VIII: 2, May 1998, pp. 28–31 and IX:1, February 1999, pp. 31–35) described two notch techniques referred to as "feedforward." In these techniques, the filter topology was modified to introduce summing junctions in the signal path and passive components were carefully selected to allow summed signals to cancel each other at specific frequencies.

Part 3 of this series describes a new notch technique, the *RC notch*, that can be broadly applied to create notches at any frequency. At the end of this series of articles, the RC notch technique will be compared to the feedforward schemes and their respective merits and drawbacks will be discussed.

The principle of the RC notch technique is shown in Figure 1, where one 2nd order section of the LTC1562 is connected as a basic all-pole 2nd order lowpass/bandpass filter and its two outputs are summed directly into the next section by means of resistor R_{IN2} and capacitor C_{IN2}.

Note that, as V_{2B} is the integral of V_{1B}, the lowpass output V_{2B} lags the bandpass output V_{1B} by 90 degrees or, conversely, V_{1B} leads V_{2B} by the same amount. Furthermore, as capacitor C_{IN2} adds another 90 degrees of phase lead to the current $I_{BP(S)}$, the two AC currents $I_{BP(S)}$ and $I_{LP(S)}$ will always be 180 degrees out of phase. It is quite trivial to show that a discrete frequency will always exist where the magnitude of these two currents will be equal and a notch will be formed.

The frequency of the notch can be easily derived by equating the magnitude of the two currents $I_{LP(S)}$ and $I_{BP(S)}$, Figure 1; that is: $I_{LP(S)} = I_{BP(S)}$

$$\text{or } V_{2B}(s)/R_{IN2} = V_{1B}(s)s\,C_{IN2} \quad (1),$$

$$\text{with } V_{2B}(s) = V_{1B}(1/(sR1C)); \quad (2);$$

$R1 = 10k$, $C = 159.15pF$, and $s = j\omega$

Substituting (2) into (1) and solving for $\omega = \omega(\text{notch}) =$

$$1/\sqrt{(R_{IN2} \bullet C_{IN2} \bullet R1 \bullet C)} \quad (3)$$

Equation 3 above can be rewritten as a function of the center frequency, f_{O1}, of the 2nd order filter section from which it was derived:

$$f_{O1} = 1/(2\pi C\sqrt{R1 \bullet R2})$$

$$f_{(NOTCH)} = f_N = f_{O1} \bullet \sqrt{(R21 \bullet C)/(R_{IN2} \bullet C_{IN2})} \quad (4)$$

Equation (4) allows a quick estimate of the notch frequency relative to the f_O. The magnitude R21 • C relative to $R_{IN2} \bullet C_{IN2}$ will determine whether the notch frequency is higher than, equal to, or lower than the

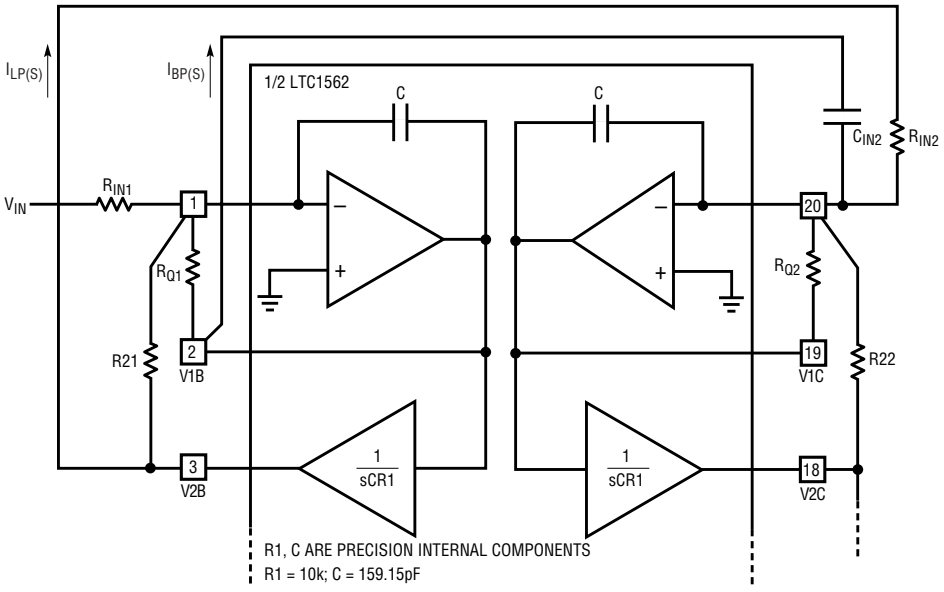


Figure 1. Summing the BP output (V1A) and the lowpass output (V1B) into the inverting node of the next LTC1562 section to form an RC notch

center frequency, f_O, of the filter section from which it was derived.

The technique of Figure 1 can be expanded to create high order filters with stopband notches. This is shown in Figure 2, where all four sections of an LTC1562 are used to create an 8th order filter. The notches, as in Figure 1, are formed by summing the two voltage outputs (V2*i*, V1*i*) via (R_{INi}, C_{INi}), respectively into the inverting node of the following section. As shown, Figure 2 supports three notches. A fourth notch can also be produced if the V_{2D}, V_{1D} outputs are summed into the inverting input of an external op amp.

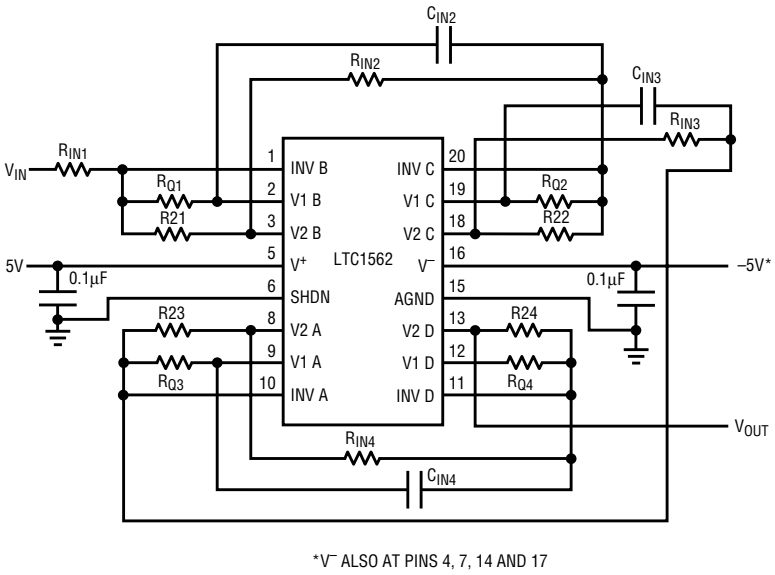
If the filter output in Figure 2 is taken from node V_{2D} and if the frequencies of all the notches are higher than the highest center frequency of any of the cascaded 2nd order sections, the overall filter response is a lowpass. As selective lowpass filters are quite popular and relatively easy to design, a lowpass example will be used to illustrate the RC notch technique. More sophisticated examples will be shown in future articles.

For the sake of thoroughness, the transfer function of Figure 2 is shown below:

$$G(s) = H \bullet \frac{\prod^{3}(s^2 + \omega^2_{Ni})\,\omega^2_{04}}{\prod^{3}(s^2 + s\omega_{0i}\alpha_i + \omega^2_{0i})} \quad (5)$$

$$\text{where } H = (R24/R_{IN1}) \bullet (C_{IN2} \bullet C_{IN3} \bullet C_{IN4})/C^3) \quad (6)$$

and where C is the internal integrator capacitor.



*V⁻ ALSO AT PINS 4, 7, 14 AND 17

Figure 2. Cascading all four sections of an LTC1562 to form an 8th order response with three notches

The DC gain of the filter is the product of the DC gains of the cascaded 2nd order sections and can be written by inspection:

$$(V_{OUT}/V_{IN}) = (R24/R_{IN4}) \bullet (R23/R_{IN3}) \bullet (R22 \bullet R_{IN2}) \bullet (R21/R_{IN1}) \quad (7)$$

An Example, Using Linear Technology FilterCAD™ for Windows®

Design a lowpass filter with a 100kHz passband and 80dB or more attenuation at 200kHz. The passband gain should be 0dB and the passband ripple should not exceed 0.2db. Use FilterCAD to synthesize the filter.

Table 1 illustrates the first try, with FilterCAD indicating a classical 7th order lowpass elliptic filter. The filter can be realized by cascading three out of four sections of the LTC1562 (Figure 3), where an external op amp is used to realize the third notch. Note the cascading sequence of 2nd order sections illustrated in Figure 3. The unused fourth section of the LTC1562 could perform another filter function, which could be independent from the above lowpass filter design.

The following step-by-step procedure shows how to calculate the external passive components of Figure 3.

1. From the LTC1562 data sheet, calculate all the R_{2i}s and R_{Qi}s:

$$R_{2i} = (100kHz/f_{0i})^2 \bullet 10k;\ R_{Qi} = Q_i \bullet \sqrt{(10k \bullet R_{2i})} \quad (8)$$
$$(i = 1, 2, 3 \ldots)$$

R21 = 17.37k; R22 = 10.387k;
R23 = 8.176k
R_{Q1} = 9.62k; R_{Q2} = 15.846k;
R_{Q3} = 49.087k

2. Calculate resistors R_{INi} and capacitors C_{INi}.

R_{INi} should be chosen independently from C_{INi} by considering DC gains; C_{INi} will be calculated to make the time constant $R_{INi} \bullet C_{INi}$ yield the appropriate notch frequency. As there are fewer commercially available capacitor values than resistors, the theoretical value of C_{INi} will be rounded

Windows is a registered trademark of Microsoft Corp.

Table 1. FilterCAD synthesis of classical 7th order elliptic response

Filter Response:	**Elliptic**		**Passband Ripple:**	**0.010dB**
Filter Type:	**Lowpass**		**Stopband Attenuation:**	**80.000dB**
Order:	**7**		**Passband Frequency:**	**100.000kHz**
			Stopband Frequency:	**200.000kHz**
f_0	**Q**	**f_N**	**Q_N**	**Type**
61.3323e3	——	——	——	LP1
75.8750e3	0.7297	204.4515e3	——	LPN
98.1197e3	1.5548	249.0337e3	——	LPN
110.5908e3	5.4287	435.4434e3	——	LPN

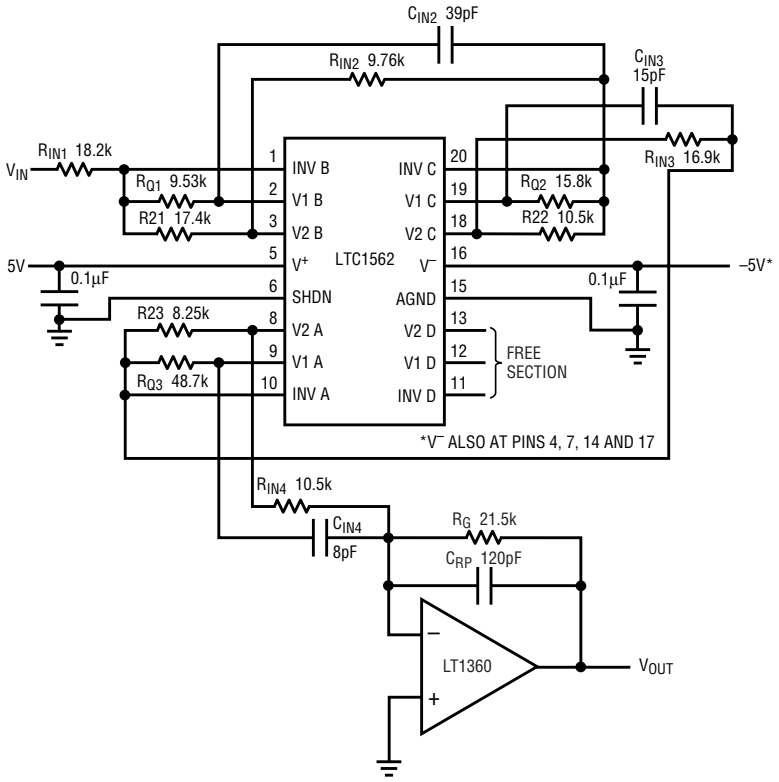


Figure 3. Cascading three sections of an LTC1562 to form a 7th order lowpass elliptic response

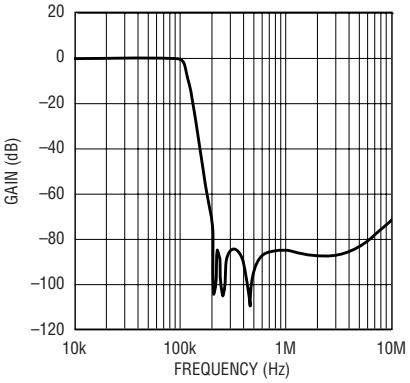


Figure 4. Measured gain response of Figure 2's circuit

off to its closest commercially available value; R_{INi} will then be appropriately adjusted to maintain the required value of the time constant $R_{INi} \bullet C_{INi}$. This algorithm is summarized below.

Set R_{INi}; Calculate C_{INi} from the notch expression (3) or (4); Round off the theoretical value of C_{INi} to the closest commercially available value; recalculate R_{INi} so that $(R_{INi} \bullet C_{INi})$ theoretical = $(R_{INi} \bullet C_{INi})$ commercially obtainable.

Optimally setting R_{INi} resistors is easier said than done. One straightforward method would allow unity DC gain at each cascaded stage, that is $R_{INi} = R_{2i}$. This could work if the filter is realized from medium Q stages (for example, Qs less than 1), but for Qs much higher than 0.707, the maximum AC gain of a lowpass 2nd order section is approximately (Q • DC gain); an internal node could have much higher gain than the filter output. This could cause internal clipping that could limit the filter's dynamic range.

A computer program can also be written to calculate the AC gain at each internal node and then make a wise choice for R_{INi} resistors. FilterCAD for Windows already performs this function for the switched capacitor products (LTC1060, LTC1061, LTC1064, LTC1067, LTC1068) and, in the near future, it will also support LTC's newer RC active products (LTC1562, et al.).

For the purpose of this article, we will use a simple rule of thumb that works fairly well, at least for lowpass elliptic filters: For Qs less than 2, set the DC gain of the second order section equal to unity, for Qs higher than 2 and less than 5, set the DC gain equal to 0.5V/V and for Qs higher than 5 and less than 8, set the DC gain equal to 0.35V/V.

2a: Set: R_{IN1} = R21 = 17.37k; this sets the DC gain of the lowpass node V21 of the first stage to 0dB.

2b: Set: R_{IN2} = R22 = 10.387k; this sets the DC gain of the lowpass node V22 with respect to V21 equal to 0db. The AC gain at V22 will peak at approximately the center frequency, f_{O2}, and the magnitude of the peak will be approximately Q2 times the DC gain. The gain at V22 with respect to V_{IN}, however, will still be close to 0dB.

Solve for C_{IN2} by using (4) above:

$$C_{IN2} = ((R21 \bullet C)/(R_{IN2})) \bullet (f_{O1}/f_{N1})^2 = 36.655pF \quad (9)$$

Choose C_{IN2} = 39pF (standard capacitor value) and readjust the value of R_{IN2}, such that

$$R_{IN2(REAL)} = (36.655pF/39pF) \bullet (10.387k) = 9.762k \quad (10)$$

2c: Set R_{IN3} = 2 • R23 = 16.352k and calculate C_{IN3} from (9) above:

$C_{IN3} = ((R22 \bullet C)/R_{IN3}) \bullet (f_{O2}/f_{N2})^2 = 15.695pF$

Choose C_{IN3} = 15pF (standard capacitor value) and readjust the value of R_{IN3} as above (10).

$R_{IN3(REAL)} = (15.695pF/15pF) \bullet (16.352k) = 17.1k$

2d: Calculate the last stage (external op amp) passive components: C_{RP}, R_G, R_{IN4} and C_{IN4}.

This is slightly more cumbersome than the previous calculations but the simple algorithm outlined below will make this task quite intuitive:

Calculate the desired ratio of R_G/R_{IN4} by considering the overall DC gain of the lowpass filter. Start with an arbitrary, yet reasonable, value for R_G, calculate R_{IN4} and also calculate C_{RP} to realize the 7th pole (real pole) of the filter (see Table 1). Make sure that the value of R_{IN4} is not too small (it should be greater than 2k). Adjust the value of R_G to accommodate a commercially available capacitor, C_{RP}.

continued on page 35

Using the LT1719 Comparator for Low Dispersion Sine Wave to Square Wave Conversion

by Joseph G. Petrofsky

The LT1719 is an UltraFast™, 4.5ns comparator with separate analog and digital supplies. Both supplies can be as low as 2.7V, or the LT1719 can be used as a level translator in mixed 3V/5V systems. The propagation delay of comparators is typically specified for a 100mV step, with some fraction of that for overdrive. But in many signal-processing applications, such as in communications, the goal is to convert a sine wave, such as a carrier, to a square wave for use as a timing clock. The desired behavior is for the output timing to be dependent only on the input timing. No dispersion or phase shift should occur as a function of the input amplitude, as this would result in AM to FM conversion. The LT1719 is an excellent choice in these applications, particularly when the input signal is larger than $100mV_{P-P}$.

Test Circuit

The circuit of Figure 1 was used to test an LT1719-based sine wave to square wave converter. The ±5V supplies on the input allow very large input swings; the 3V logic supply keeps the output swing small to minimize coupling back into the inputs. Characterization of the delay, which varies just a fraction of a nanosecond over a decade of input amplitude change, is not simple. A fast oscilloscope can have ±500ps of variation in any given channel. This can be calibrated by swapping input and output channels and averaging the readings if the two signals allow the same vertical scale factors. But for a measurement of delay changes over a decade or more of amplitude range, accuracy is degraded by delay dependence on the gain settings of the oscilloscope's vertical path.

To characterize the delay, an HP4195 Spectrum/Network Analyzer was used to look at the phase of the output relative to the input (Test/Ref). Because the HP4195 is a spectrum/network analyzer, it can reject the harmonics of the output square wave, unlike some network-only analyzers. The phase of the fundamental component of the LT1719 output can be slightly affected by the exact nature of any overshoot or undershoot of the transitions, so a pair of antiparallel diodes is used to clip off these portions of the output waveform. The rest of the circuitry on the output is a filter whose exact behavior does not affect the measurement because the same amplitude and frequency signal will always be present there and only relative changes in phase will be examined.

The input signal is terminated in a resistive –12dB pad that creates the reference signal for the analyzer. The HP4195 maximum oscillator level is 15dBm or $3.56V_{P-P}$. The 1:2 transformer steps this up to $7.12V_{P-P}$ differential at the DUT input. An amplifier could be used to boost the amplitude further, but distortion in the amplifier could result in phase errors because the LT1719 will respond to the zero-crossings, whereas the HP4195 will respond to the phase of the fundamental. The results without a transformer, grounding the unused comparator input, were unchanged but for the loss of 6dB.

Results

Figure 2 shows the time delay of the sine wave to square wave converter responding to an amplitude sweep at 10MHz. The delay is calculated as:

$$t_{DELAY} = t_{DELAY}|_{0dBm} - \frac{(\theta - \theta|_{0dBm})}{360^\circ \bullet 10MHz}$$

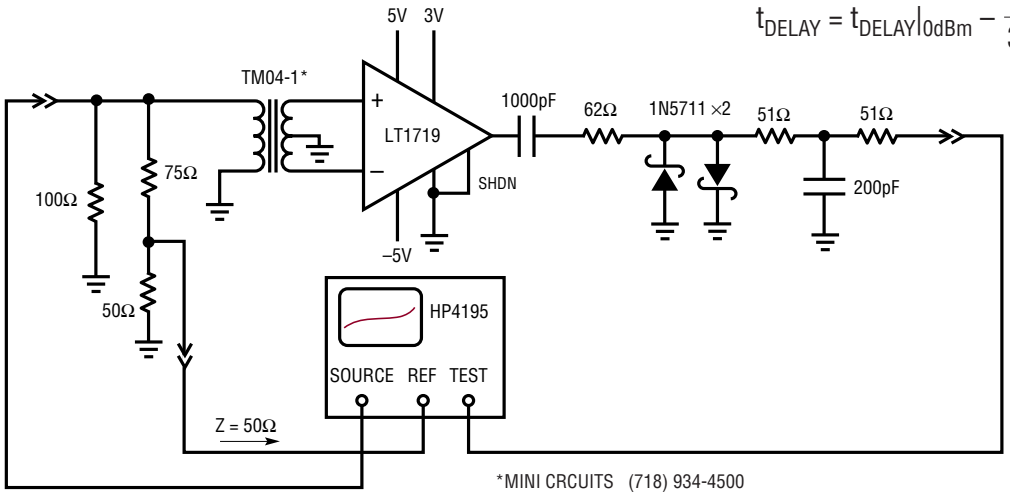


Figure 1. Sine to square wave converter schematic

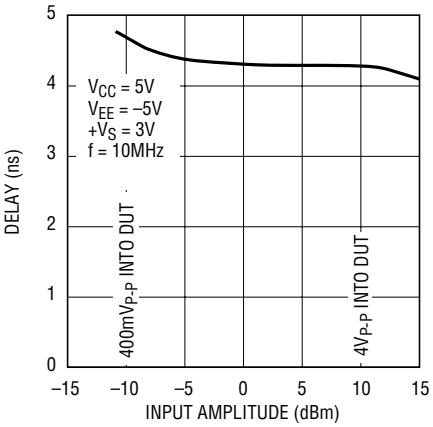


Figure 2. Time delay vs sine wave input amplitude

where θ is the phase in degrees measured by the network analyzer and $t_{DELAY}|_{0dBm}$ is the absolute delay at 0dB input amplitude, which was measured with a fast oscilloscope using the calibration method described earlier. The LT1719 delay changes just 0.65ns over the 26dB amplitude range; 2.33 degrees at 10MHz. The delay is particularly flat, yielding excellent AM rejection, from –5dBm to 10dBm, a common range for RF signal levels.

With small input signals, the hysteresis of the LT1719 (3.5mV typ.) and increased propagation delay make the LT1719 act like a comparator with a 12mV hysteresis span. In other words, a $12mV_{P-P}$ sine wave at 10MHz will barely toggle the LT1719, but with 90° of phase lag or 25ns additional delay. Above $5V_{P-P}$ at 10MHz, the LT1719 delay starts to decrease due to the internal capacitive feedforward in the design of the input stage. Unlike some comparators, the LT1719 will not falsely anticipate a change in input polarity, but the feedforward is enough to make a transition propagate through the LT1719 faster once the input polarity does change.

At frequencies higher than 10MHz, attention to detail in the physical construction of circuits becomes particularly important. With a poor layout, the output toggle action can capacitively or inductively couple back to the input signal, causing distortion. This must be avoided in order to measure the actual performance of the comparator. The LT1719 pinout has been optimized to shield the input signals from the digital signals with two intervening power supply pins.

Conclusion

The new LT1719 comparator can easily be used to create a low power, high performance, sine wave to square wave converter. The fast, 4.5ns delay barely changes with input amplitude fluctuations. The delay is particularly flat, for excellent AM rejection, from –5dBm to 10dBm.

LTC1562 notches, continued from page 33

Calculate C_{IN4} as in the previous steps and adjust the value of R_{IN4}. The choice of capacitors will most likely alter the original ratio of R_G/R_{IN4}, so readjust the value of the input resistor R_{IN1} to restore the DC gain of the filer to its original value.

2d-1. Set the overall gain of the lowpass filter to its desired value (here we are assuming 1V/V) and calculate the ratio of R_G/R_{IN4}:

$$(V_{OUT}/V_{IN})\ DC = (R_G/R_{IN4}) \bullet (R23/R_{IN3}) \bullet (R22/R_{IN2}) \bullet (R21/R_{IN1}) = 1V/V \quad (11)$$

$R_G/R_{IN4} = 1.9656$

2d-2. Start with an arbitrary, yet reasonable value, for example R_G = 20k, and solve for C_{RP} to obtain the 7th real pole frequency of 61.332kHz.

C_{RP} = 129.75pF; choose C_{RP} = 120pF and adjust R_G to 21.625k

Solve for $R_{IN4} = R_G/1.956 = 11.05k$

2d-3. Calculate $C_{IN4} = ((R23 \bullet C)/R_{IN4}) \bullet (f_{O3}/f_{N3})^2 = 7.595pF$

Choose C_{IN4} = 8pF (standard value) and readjust R_{IN4} to

$R_{IN4(REAL)} = (7.595pF/8pF) \bullet (11.05k) = 10.49k$

2d-4 As the new ratio (R_G/R_{IN4}) has changed slightly [$(R_G/R_{IN4})_{REAL}$ = 2.06 instead of 1.9656], adjust R_{IN1} to reestablish 0dB of DC gain: $R_{IN1(REAL)} = 17.37k \bullet (2.06/1.9656) = 18.2k$.

Experimental Results

The resistor values derived above are first rounded off to their nearest 1% values, as shown below:

1% surface mount resistors, type 0805:

R_{IN1} = 18.2k, R21 = 17.4k, R_{Q1} = 9.53k
R_{IN2} = 9.76k, R22 = 10.5k, R_{Q2} = 15.8k
R_{IN3} = 16.9k, R23 = 8.25k, R_{Q3} = 48.7k
R_{IN4} = 10.5k, R_G = 21.5k

The choice of the above 1% values increases the DC gain by 0.24dB so the value of R_{IN1} is raised from 18.2k to 18.7k (1%) to restore the 0dB value of the passband gain.

Resistors R_{Q2} and R_{Q3} are also slightly changed to predistort the values of Q2 and Q3, as shown in the LTC1562 data sheet curve (Q error vs nominal f_O). This is done by lowering the values of R_{Q2} and R_{Q3} by the same percentages as the Q error. The new values are R_{Q2} = 15k (1%) and R_{Q3} = 45.3k (1%).

The filter of Figure 2 was constructed with the resistor values shown above and with 5% type X7R surface mount capacitors:

C_{IN2} = 39pF, C_{IN3} = 15pF, C_{IN4} = 8pF, C_{RP} = 120pF

The active devices are the LTC1562A and the LT1360 op amp. Figure 4 shows the filter gain response. The measured passband error is 0.15dB and the total output RMS noise is $60\mu V_{RMS}$. With a dual 5V supply, the filter can easily provide a 5V peak-to-peak signal with a 90dB signal-to-noise ratio and better than 0.01% distortion. The attenuation of the filter remains below 80dB for input frequencies up to 6MHz.

Conclusion

A simple method of how to systematically synthesize and design a high performance lowpass elliptic filter is fully illustrated above. The experimental results match the theoretical calculations provided; the Q-setting resistors are slightly adjusted to account for the small Q errors of the LTC1562A.

LT1461, continued from page 5

This is pretty hard to determine (read impossible) if the peak-to-peak output noise is larger than this number. As a practical matter the best laboratory reference available has long-term drift of 1.5µV/mo. This performance is only available from the very best subsurface Zener references using specialized heating techniques.

The LT1461 long-term drift data was taken with parts that were soldered onto PC boards as in a "real world" application. The boards were then placed in a constant-temperature oven with T_A = 30°C and their outputs were scanned regularly and measured with an 8.5 digit DVM. Figure 4 shows the long-term drift of three typical LT1461S8-2.5s soldered into a PC board. This is the best performance we have measured on an IC voltage reference that is not based on a subsurface Zener.

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Conclusion

The LT1461 series reference meets the growing need for low power, high accuracy and low temperature coefficient, while simultaneously serving micropower precision regulator applications. This new bandgap reference comes in the 8-lead SO package. It is available in 2.5V and will be available in 4.096V, 5.0V and 10V options.

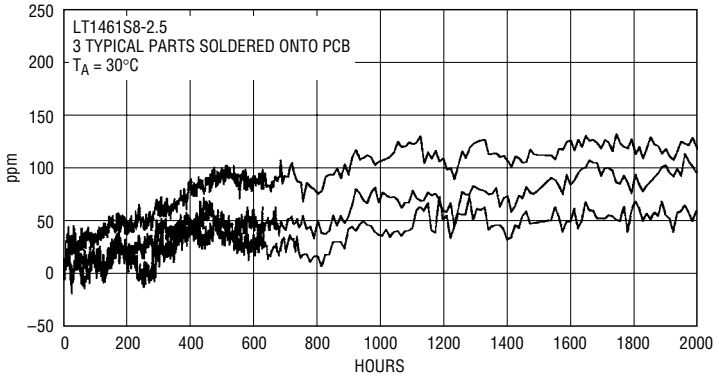

Figure 4. Long-term drift

LTC1929, continued from page 28

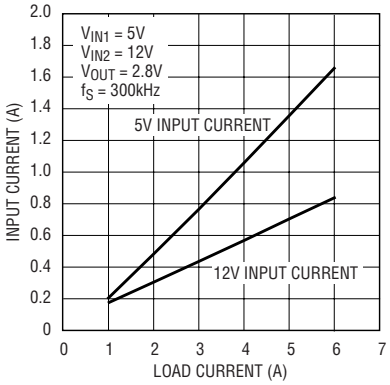

Figure 2. Input currents vs load current for Figure 1's circuit

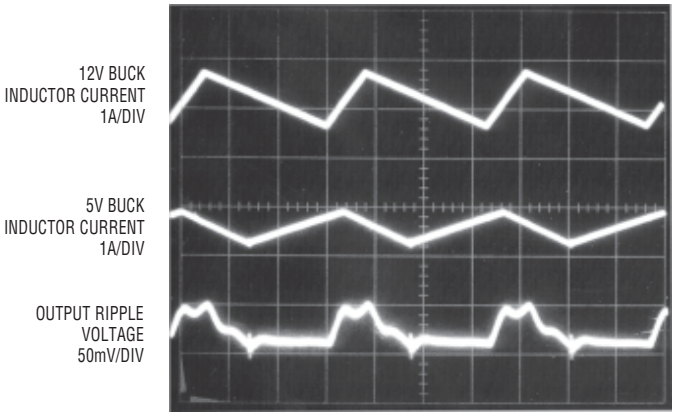

Figure 3. Ripple current and voltage waveforms

Figure 1 shows the schematic diagram of the complete power supply. The switching frequency is about 300kHz per-channel for an effective output ripple frequency of 600kHz. The inductors in both stages are 7µH. The current sense resistor is 0.007Ω for each channel.

Test Results

The overall efficiency is above 90% from 0.5A to 6A. Figure 2 shows the distribution of two input currents as the load current varies. The maximum input currents for the 5V and 12V sources are 1.66A and 0.84A, respectively, which are well below the PCI connector's current limits. Figure 3 shows the waveforms of the inductor ripple currents and output ripple voltages. Note the ripple cancellation phenomenon. The peak-to-peak switching ripple voltage at the output terminal is only 50mV$_{P-P}$ with one 1500µF/6.3V aluminum electrolytic capacitor. If two buck circuits are synchronized in phase, the ripple voltage will be 70mV$_{P-P}$, almost a 50% increase.

Conclusion

The PolyPhase technique reduces the output ripple voltage without increasing the switching frequency. High efficiency can be obtained for low output voltage applications. The LTC1929 PolyPhase controller provides a small, low cost solution for multi-input applications. If more than two inputs are needed, use the LTC1629 rather than the LTC1929. Multiple LTC1629s can be configured for 3-, 4-, 6- or even 12-phase operation.

New Device Cameos

LT1637: Rugged Rail-To-Rail Op Amp Delivers 1.1MHz Gain-Bandwidth Product from 250µA Supply Current

The LT1637 is a rugged op amp; it has Over-the-Top inputs, rail-to-rail output, shutdown and reverse supply protection. The LT1637 achieves a gain-bandwidth product of 1.1MHz while drawing less than 250µA of quiescent current and operates on all single and split supplies with a total voltage of 2.7V to 44V. The output of the LT1637 will swing to within 3mV of V^- with less than 1mV of input overdrive, making it ideal for sensing voltages close to ground in single-supply systems. The LT1637 is easily shut down, with a shutdown pin current of less than 5µA. In shutdown, the LT1637's output is high impedance and its quiescent current drops to only 3µA. The LT1637 draws virtually no current for reverse supplies of up to 25V. Unlike most micropower op amps, the LT1637 can drive heavy loads: its rail-to-rail output drives 25mA. The LT1637 is unity-gain stable into all capacitive loads up to 220pF (4700pF when 0.22µF and 150Ω compensation is used).

The LT1637 has a unique input stage that operates and remains high impedance when above the positive supply. The inputs take 44V both differential and common mode, even when operating on a 3V supply. Built-in resistors protect the inputs for faults below the negative supply up to 22V. There is no phase reversal of the output for inputs 5V below V_{EE} or 44V above V_{EE}, independent of V_{CC}.

The LT1637 op amp is available in the 8-pin MSOP, 8-pin SO and PDIP packages.

The LTC1655L: Smallest 16-Bit Voltage-Output DAC Saves Board Space

The LTC1655L is the smallest 16-bit voltage-output DAC available today. It is available in an 8-pin SO package and includes an internal 1.25V reference and a rail-to-rail voltage output amplifier. The LTC1655L is guaranteed to be monotonic over the industrial temperature range with a typical differential nonlinearity of 0.3LSB. It is pin compatible with Linear Technology's 12- and 14-bit DAC family, allowing an easy upgrade path. The LTC1655L can operate on a wide supply range of 2.7V to 5.5V, dissipating 1.6mW from a 3V supply. The output swings from 0V to 2.5V when using the internal reference. The reference pin can be overdriven to a higher voltage for a wider output swing.

The LTC1655L has a flexible, SPI/QSPI and MICROWIRE™ compatible, 3-wire serial interface. A D_{OUT} pin allows daisy chaining. The SCK pin is equipped with an internal Schmitt trigger for noise immunity, allowing direct optocoupler interfacing to the part. The logic inputs are TTL level compatible. The rail-to-rail voltage output will swing to within a few millivolts of either supply rail when unloaded and is capable of driving capacitive loads of up to a 1000pF without oscillating.

LTC1798 Low Dropout References Draw Only 6.5µA of Supply Current

The LTC1798-2.5, LTC1798-3, LTC1798-4.1 and LTC1798-5 are 6.5µA series voltage references with guaranteed 0.15% accuracy, a maximum of 40ppm/°C temperature drift and 200mV dropout voltage that do not require an output capacitor for stability. An adjustable version, the LTC1798, is also available.

This family of references operates on supplies as high as 12.6V. They can source up to 10mA and sink up to 2mA, making them ideal for precision regulator applications. They use trimmed thin-film resistors and curvature compensation to achieve high output accuracy and low temperature coefficient.

MICROWIRE is a trademark of National Semiconductor Corp.

The LTC1798 family of series references provides supply current and power dissipation advantages over shunt references that must idle the entire load current to operate. The LTC1798 series is available in the 8-pin SO package.

LTC1647 Device-Bay Chip Hot Swaps Peripherals

The LTC1647 dual Hot Swap controller allows a board to be safely inserted into and removed from a live backplane. Equally at home on either side of the connector, the LTC1647 can act from the host side or reside on the hot swappable product. It is particularly well suited for USB and Device Bay applications.

The two sections of the LTC1647 operate independently and each features an electronic circuit breaker, a fault flag and an ON/OFF control that doubles as a programmable undervoltage lockout. Each section drives an N-channel pass transistor, allowing any two supply voltages from 2.7V to 15V to be ramped at a controlled rate. The LTC1647 operates under the control of a microprocessor or autonomously, including recovering from fault conditions.

Several package options offer a choice of control and fault pin configurations; 8-pin SO and 16-lead SSOP packages are available.

LT1812: 3mA, 100MHz, 750V/µs Operational Amplifier with Shutdown

The LT1812 is a low power, high speed, very high slew rate operational amplifier with excellent DC performance. Compared to other devices with similar bandwidth, the LT1812 features reduced supply current, lower input offset voltage (0.5mV typical) and lower input bias current (1µA typical). A power-saving shutdown feature reduces supply current to 50µA. The circuit topology is a voltage feedback amplifier with the slewing characteristics of a current feedback amplifier. Both inputs are high impedance, like those of a voltage feedback amplifier. However, the slew rate is a function of the input step as well as the gain

configuration, much like a current feedback amplifier.

The LT1812 is specified at both ±5V and with a single 5V supply. The input common mode range is symmetrical at ±3.5V minimum (±5V supply) and at1.5V–3.5V minimum for a single 5V supply. The output drives a 100Ω load to ±3.5V with ±5V supplies. On a single 5V supply, the output swings from 1.1V to 3.9V with a 100Ω load connected to 2.5V. The amplifier is stable over a wide range of capacitive loads, from no load to 1000pF, which makes it useful in buffer and cable-driver applications.

The LT1812 is available in the 8-pin SO package.

LT1721 Quad, 4.5ns, Comparator in an SO-8 Sized Package Works Down to 2.7V

The LT1721 is an UltraFast™ quad comparator optimized for single-supply operation with a supply voltage range of 2.7V to 6V. The LT1721 is offered in the 16-lead SO package, as well as the 16-lead GN, which is the same size as an SO-8.

Propagation delay is just 4.5ns typical (6.5ns max) with 20mV overdrive and 7ns typical (10ns max) with 5mV overdrive. Quiescent current is only 4mA typical (7mA max) per comparator. The input voltage range extends from 100mV below ground to 1.2V below the supply voltage. Phase-reversal circuitry prevents false output states when the inputs are driven even further below ground.

Internal hysteresis makes the LT1721 easy to use even with slowly moving input signals. Input DC specifications feature an offset voltage of 1mV typical (3mV max.) with full-temperature range limits on all DC specifications including input hysteresis and trip points. The rail-to-rail outputs can directly interface to TTL and CMOS. Alternatively, their symmetric output drive can be harnessed for analog applications or easy translation to other logic levels.

The LT1721 is a quad version of the LT1720 dual comparator. These products, along with the LT1719 single comparator, constitute an easy-to-use, high speed comparator family that features small size, low power, and low cost.

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DESIGN TOOLS

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DESIGN TOOLS, continued from page 39

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